20170125.1526.0107

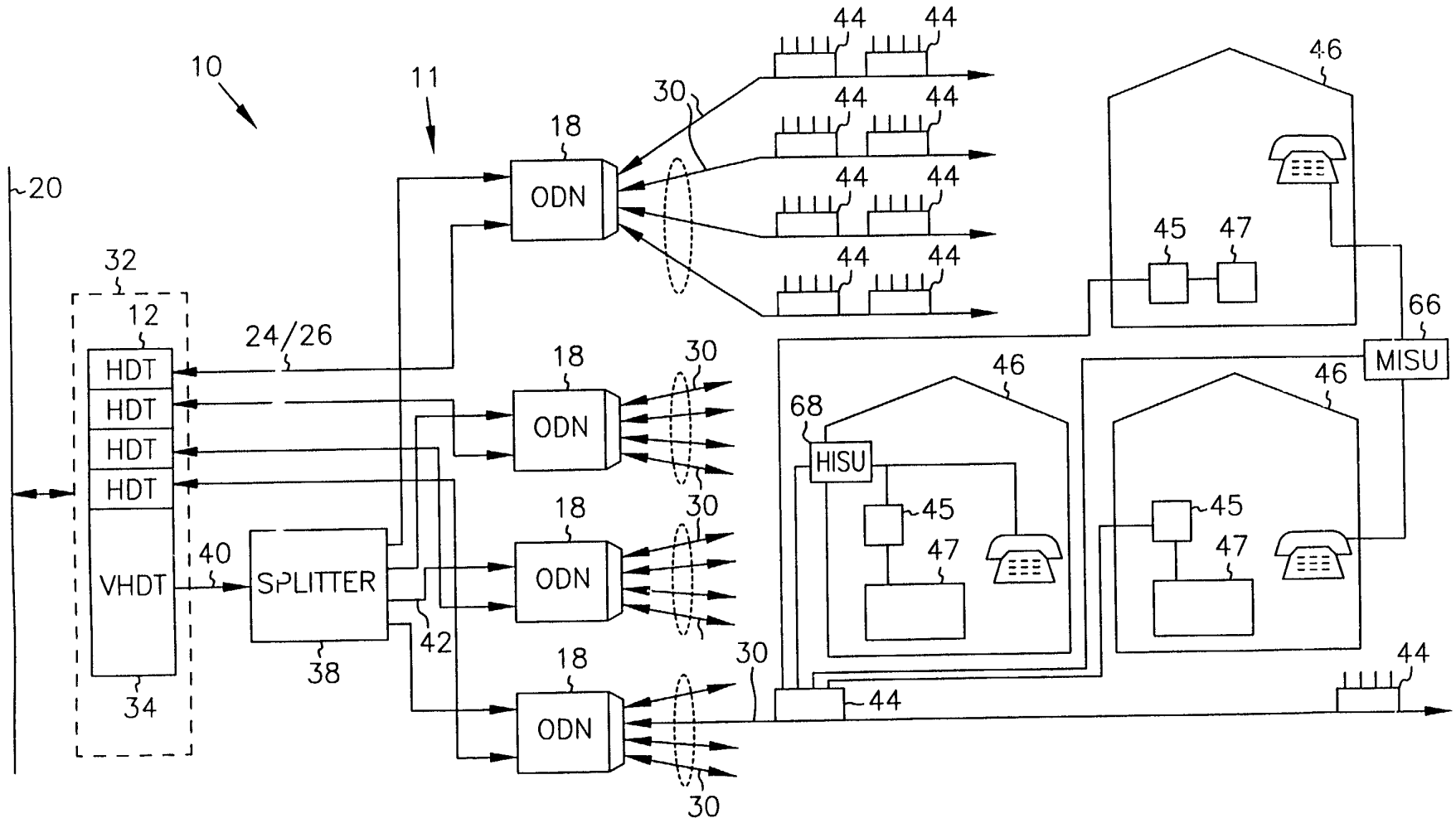


FIG. 1

PRINTED SCREEN

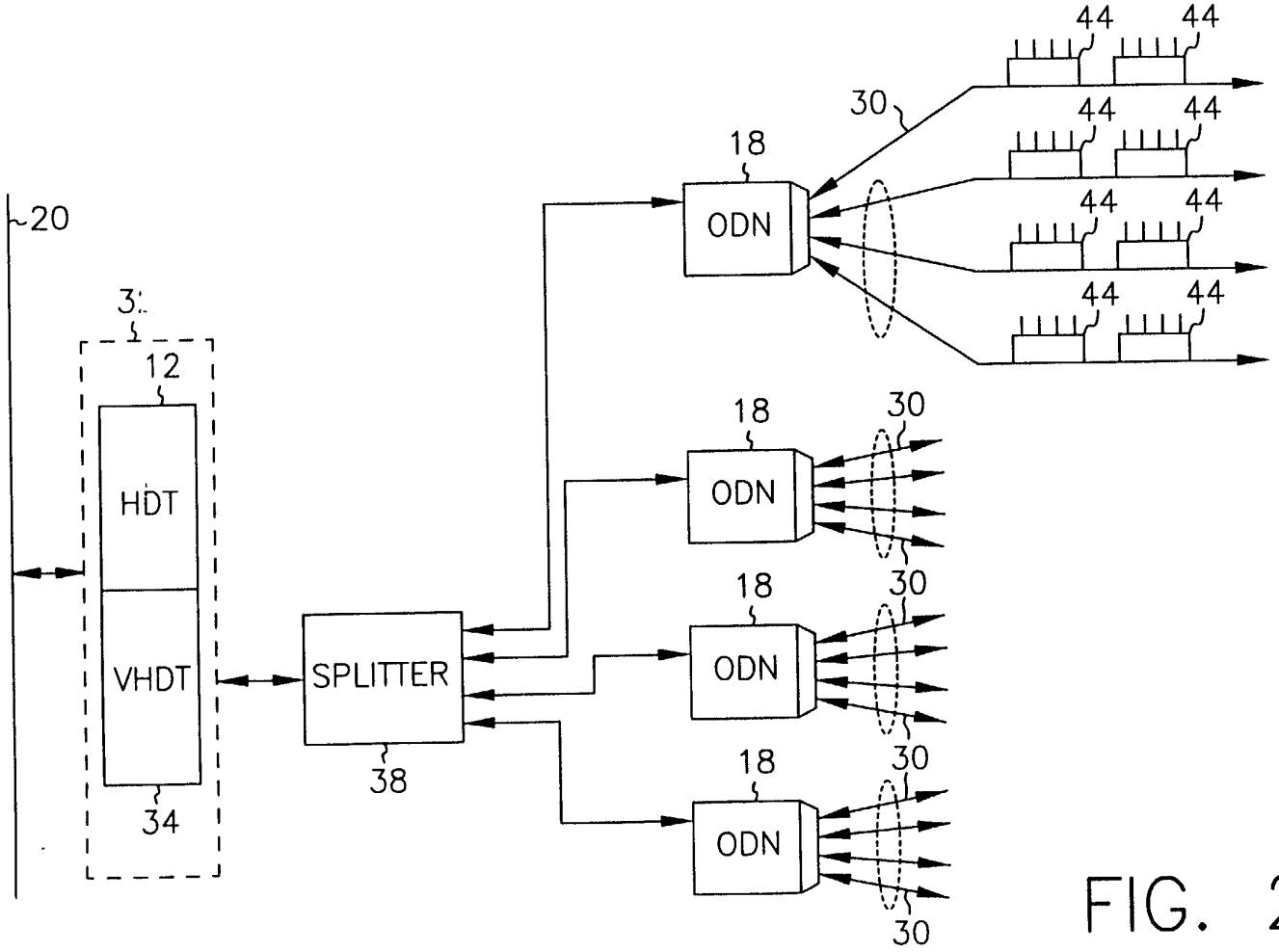


FIG. 2

20170 ES2618T

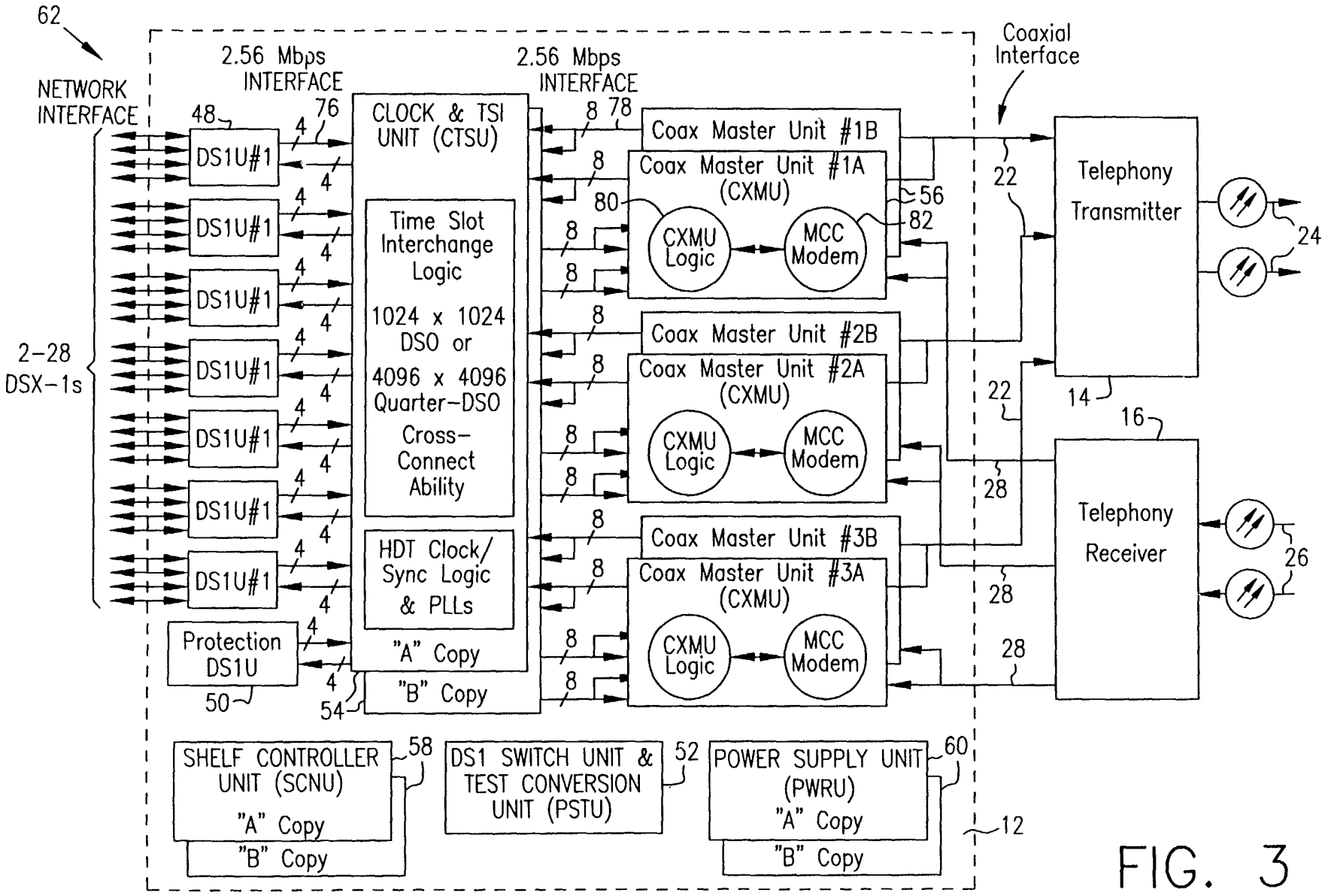
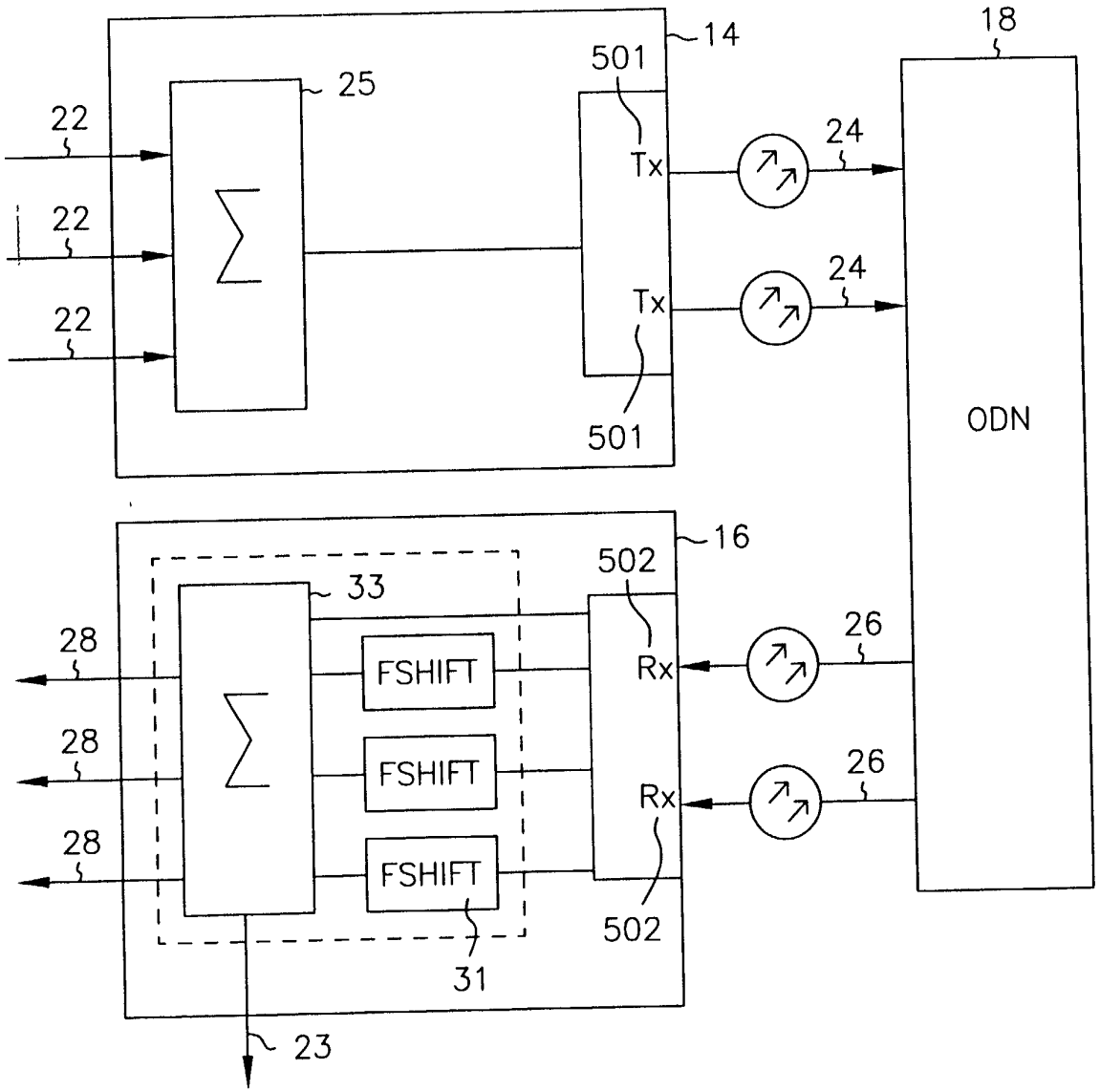


FIG. 3

20170125204807

FIG. 4



20170-2526.001

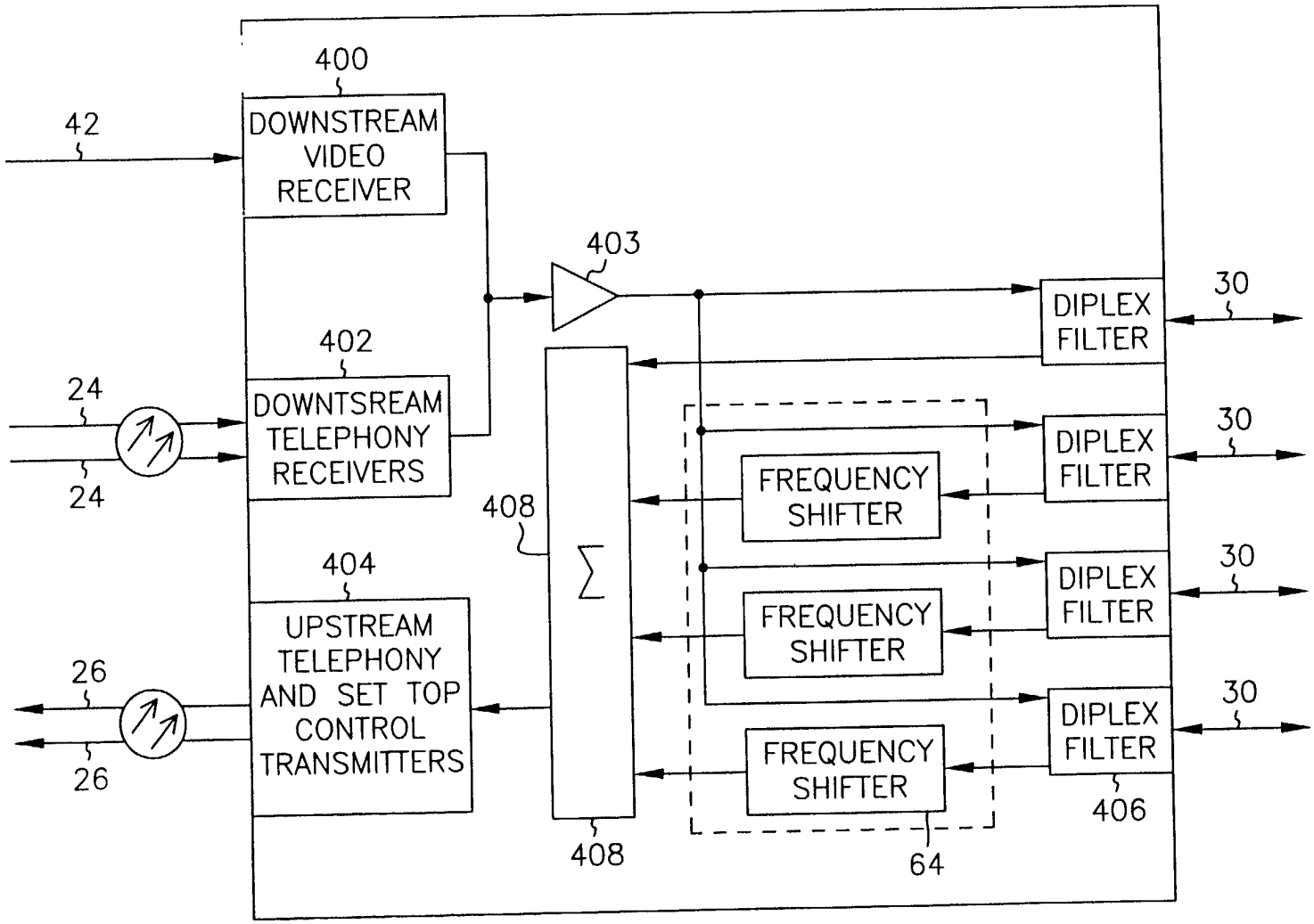


FIG. 5

DO NOT ENTER

FIG. 6

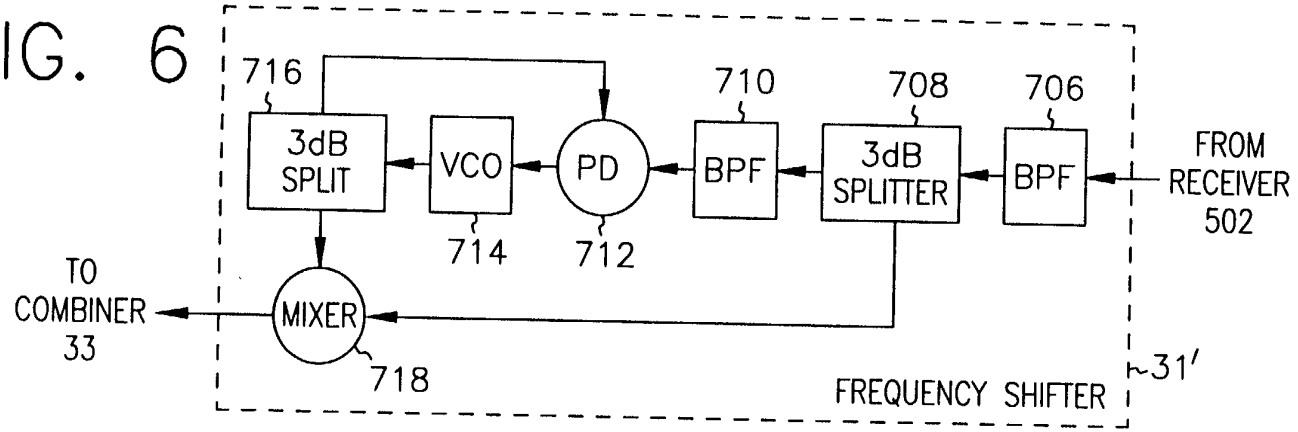
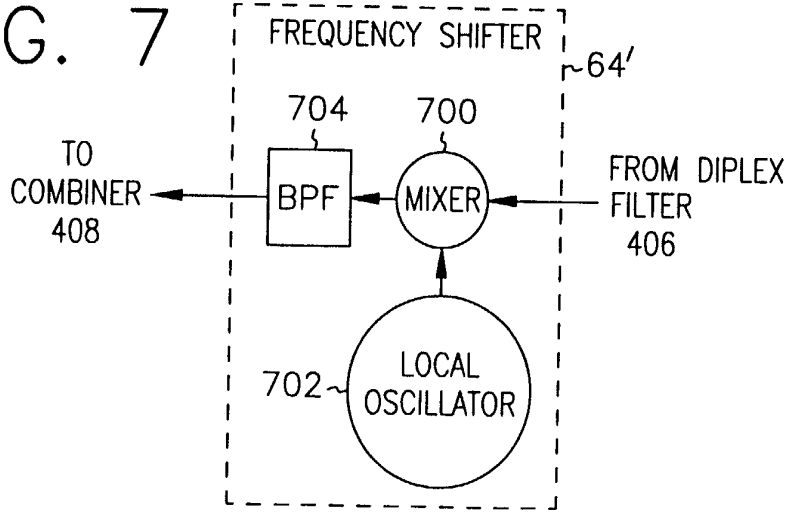


FIG. 7



20170815280T

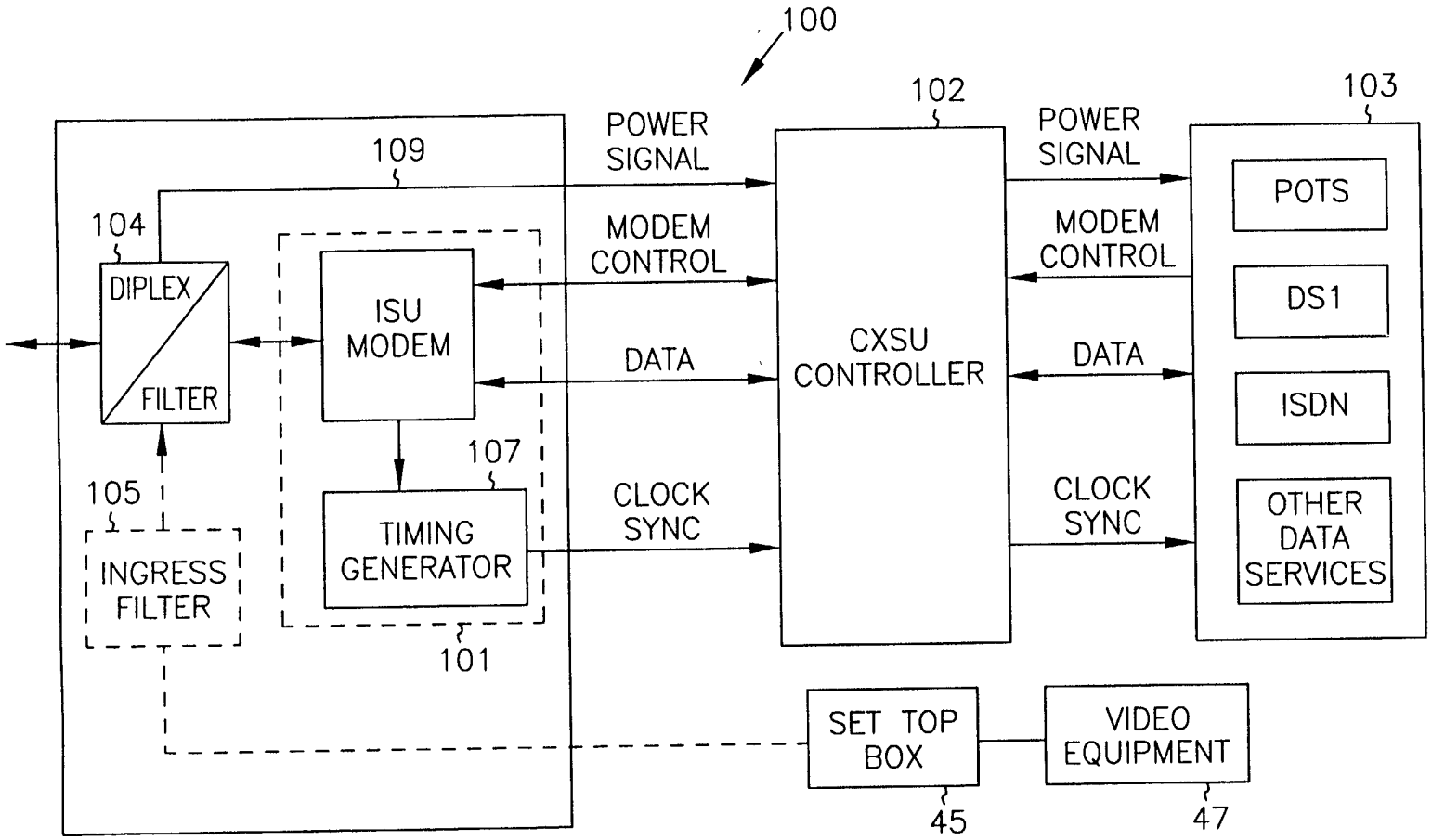


FIG. 8

SCHEDULE

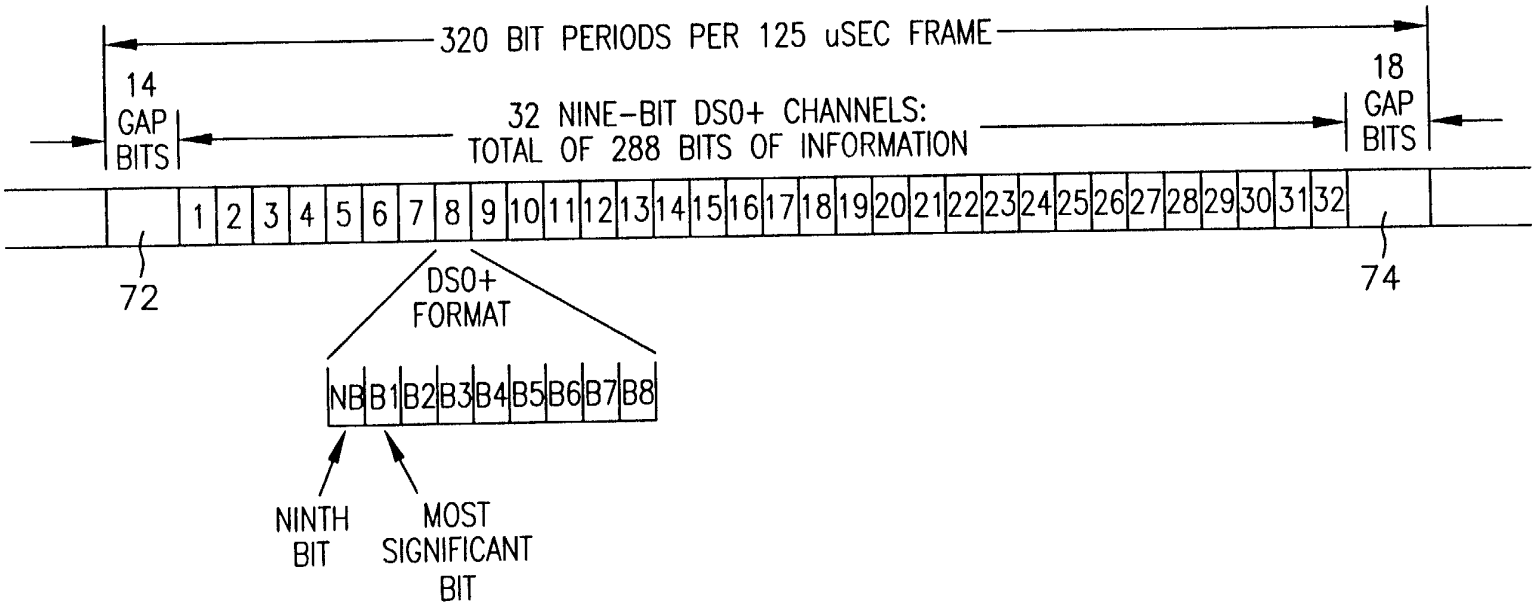


FIG. 9

SOFTSCAN

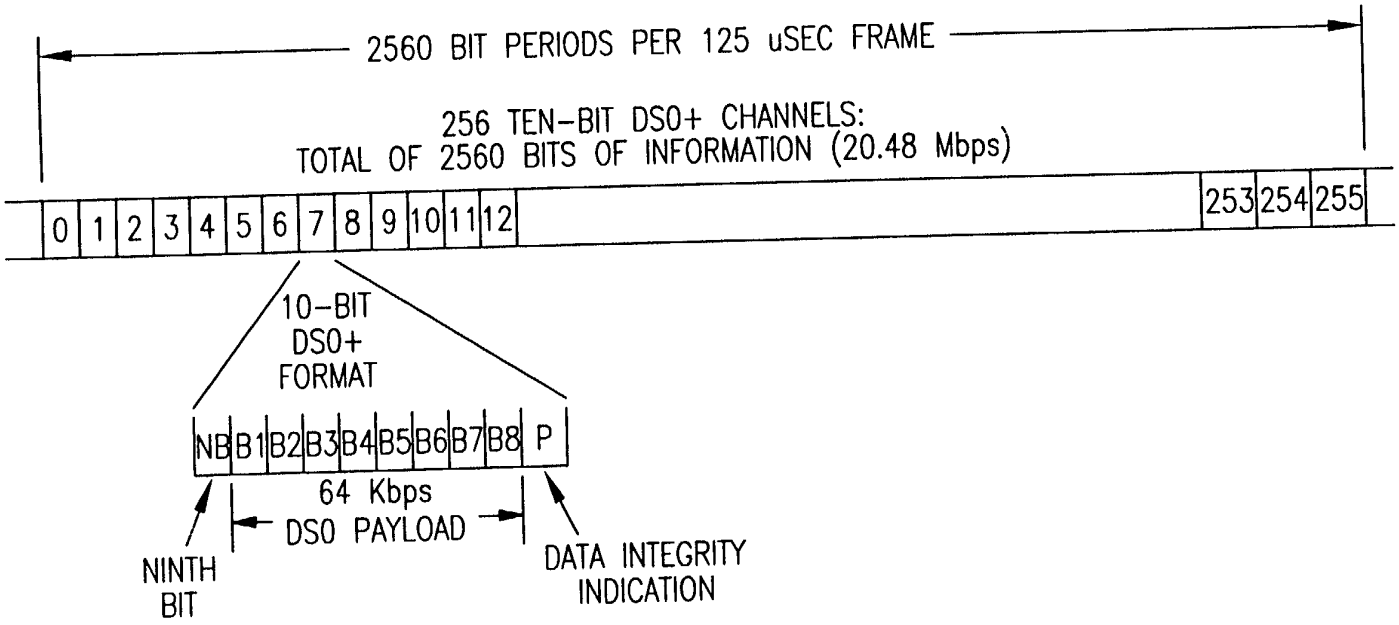


FIG. 10

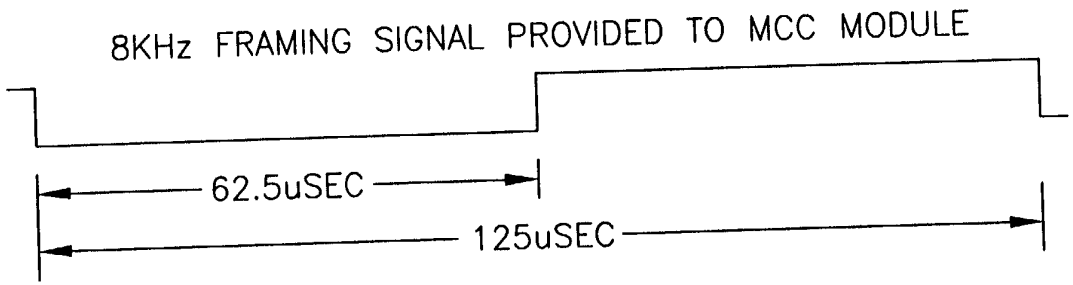

8KHz FRAMING SIGNAL PROVIDED TO MCC MODULE
62.5uSEC
125uSEC

FIG. 11

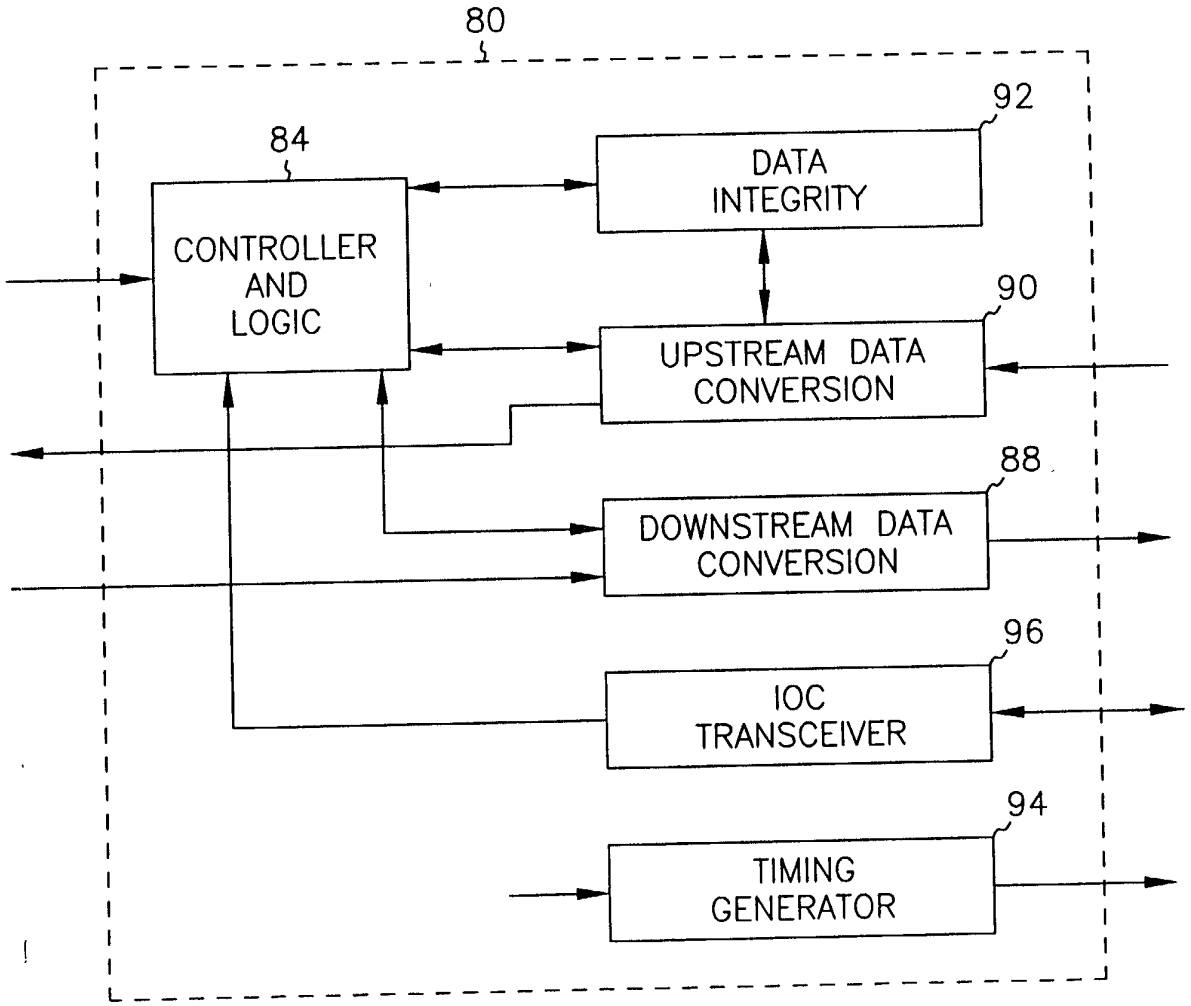

80
84
CONTROLLER AND LOGIC
92
DATA INTEGRITY
90
UPSTREAM DATA CONVERSION
88
DOWNSTREAM DATA CONVERSION
96
IOC TRANSCEIVER
94
TIMING GENERATOR

FIG. 12

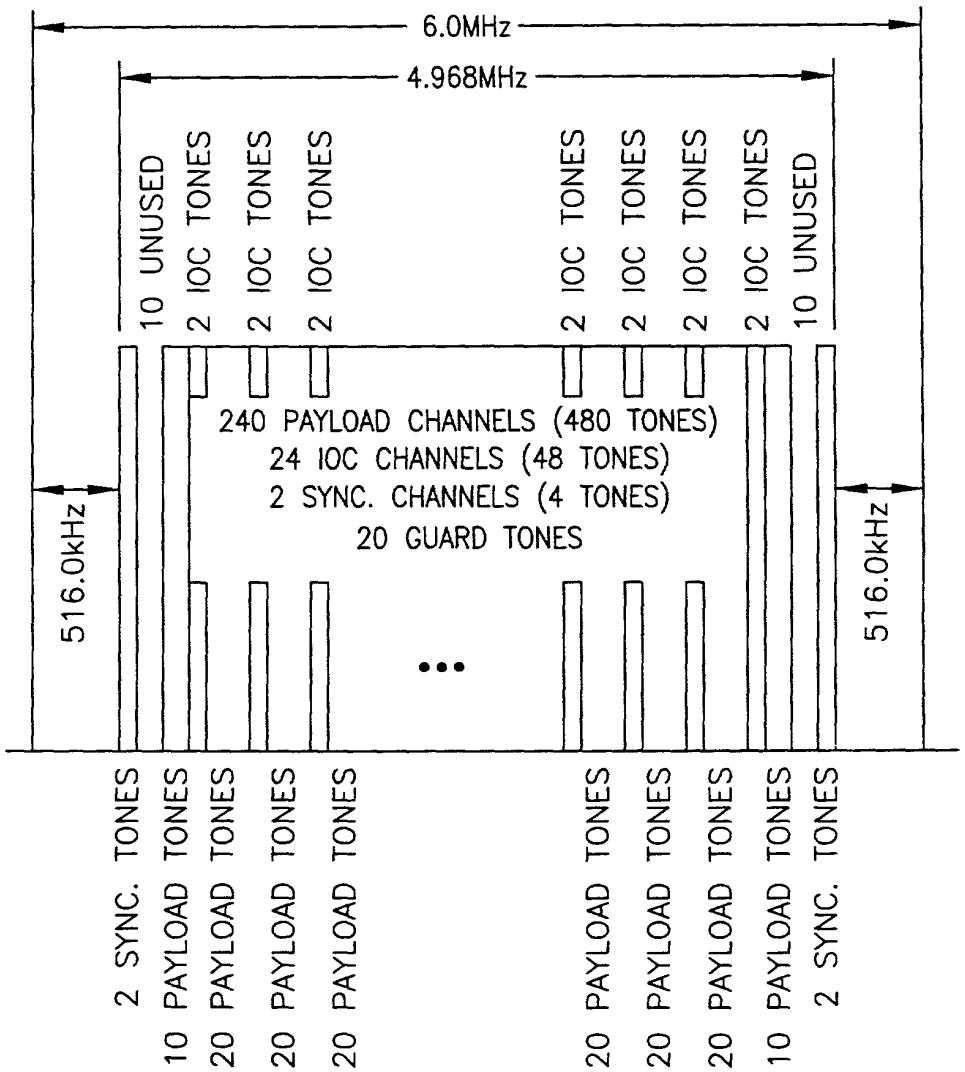

6.0MHz
4.968MHz
10 UNUSED
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
2 IOC TONES
10 UNUSED
240 PAYLOAD CHANNELS (480 TONES)
24 IOC CHANNELS (48 TONES)
2 SYNC. CHANNELS (4 TONES)
20 GUARD TONES
516.0kHz
516.0kHz
2 SYNC. TONES
10 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
20 PAYLOAD TONES
10 PAYLOAD TONES
2 SYNC. TONES

FIG. 13

Approved for Release: 2025/07/08

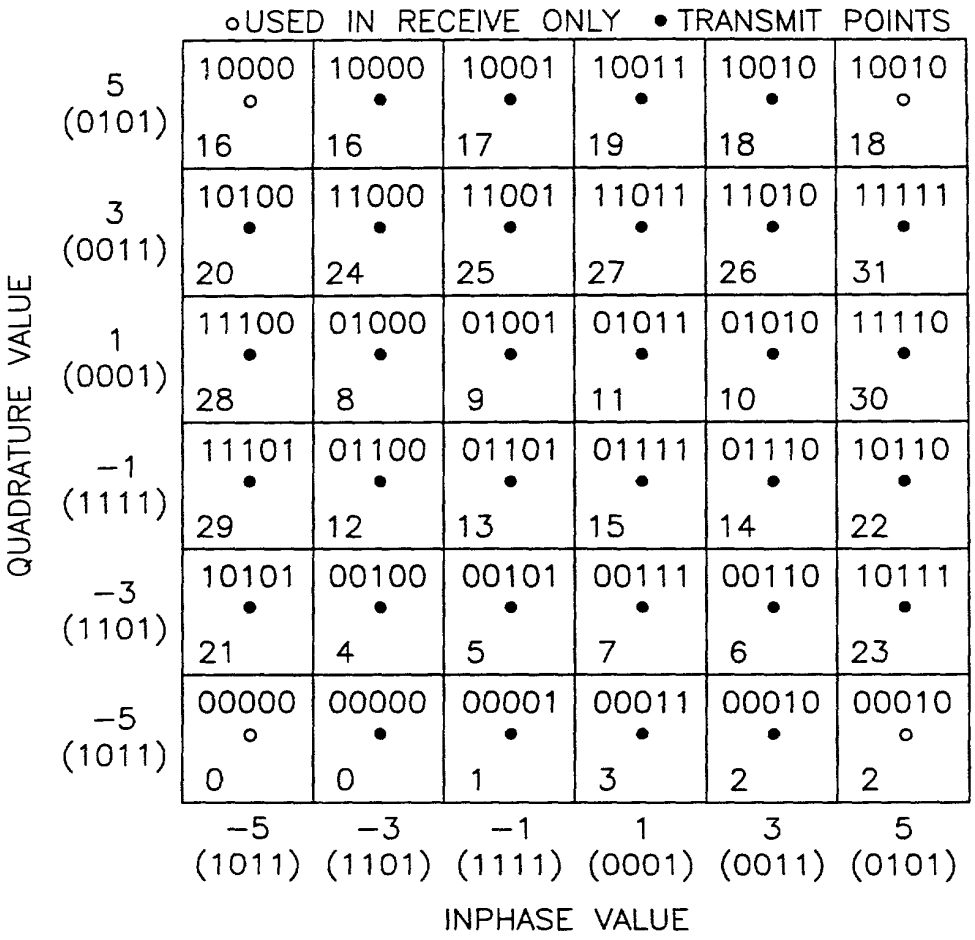


FIG. 14

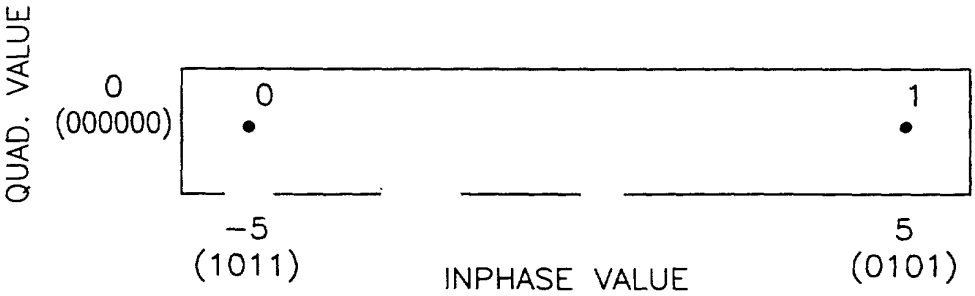


FIG. 15

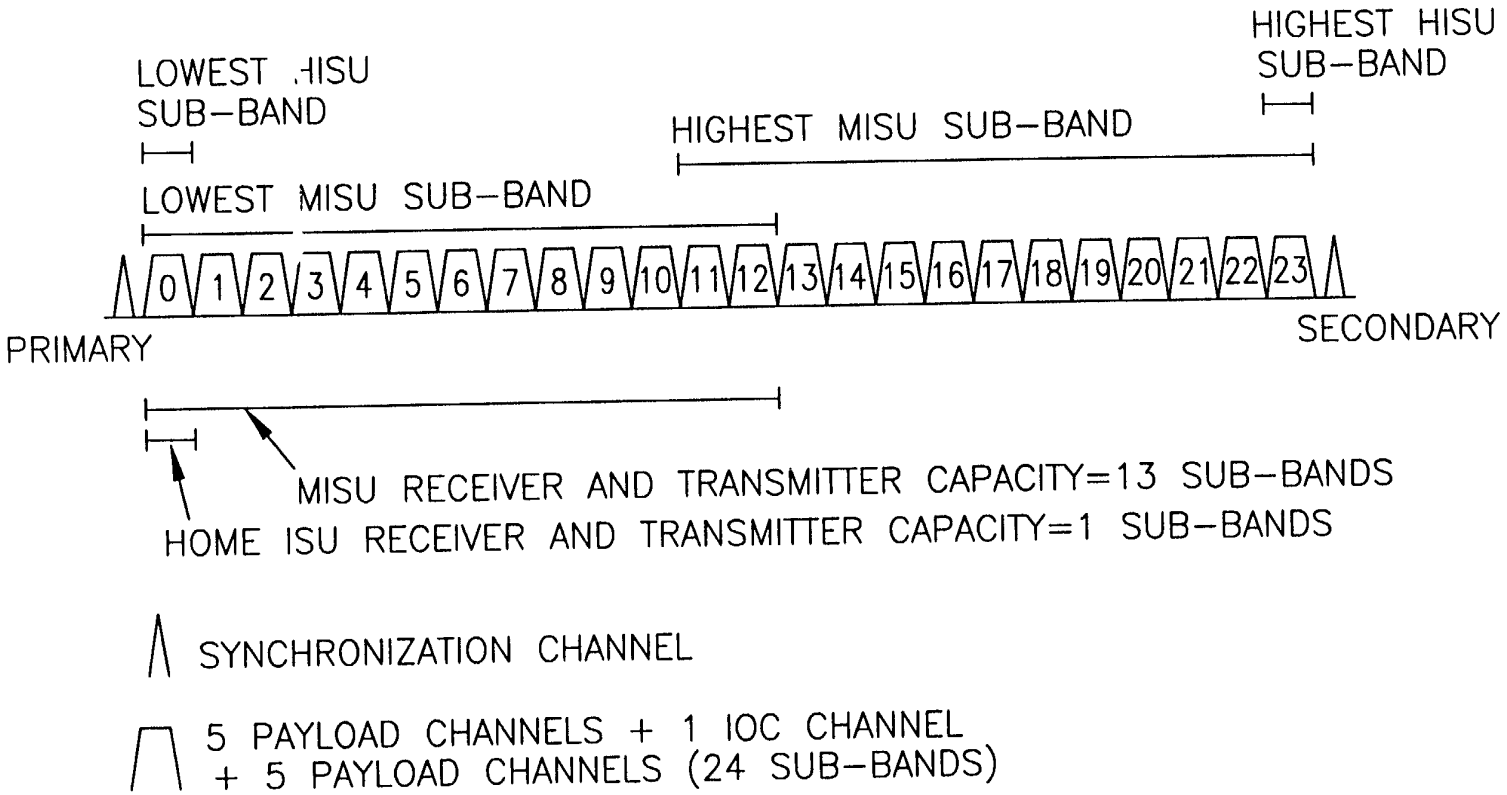

HIGHEST HISU
SUB-BAND
LOWEST HISU
SUB-BAND
HIGHEST MISU SUB-BAND
LOWEST MISU SUB-BAND
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
PRIMARY
SECONDARY
MISU RECEIVER AND TRANSMITTER CAPACITY=13 SUB-BANDS
HOME ISU RECEIVER AND TRANSMITTER CAPACITY=1 SUB-BANDS
SYNCHRONIZATION CHANNEL
5 PAYLOAD CHANNELS + 1 IOC CHANNEL
+ 5 PAYLOAD CHANNELS (24 SUB-BANDS)

FIG. 16

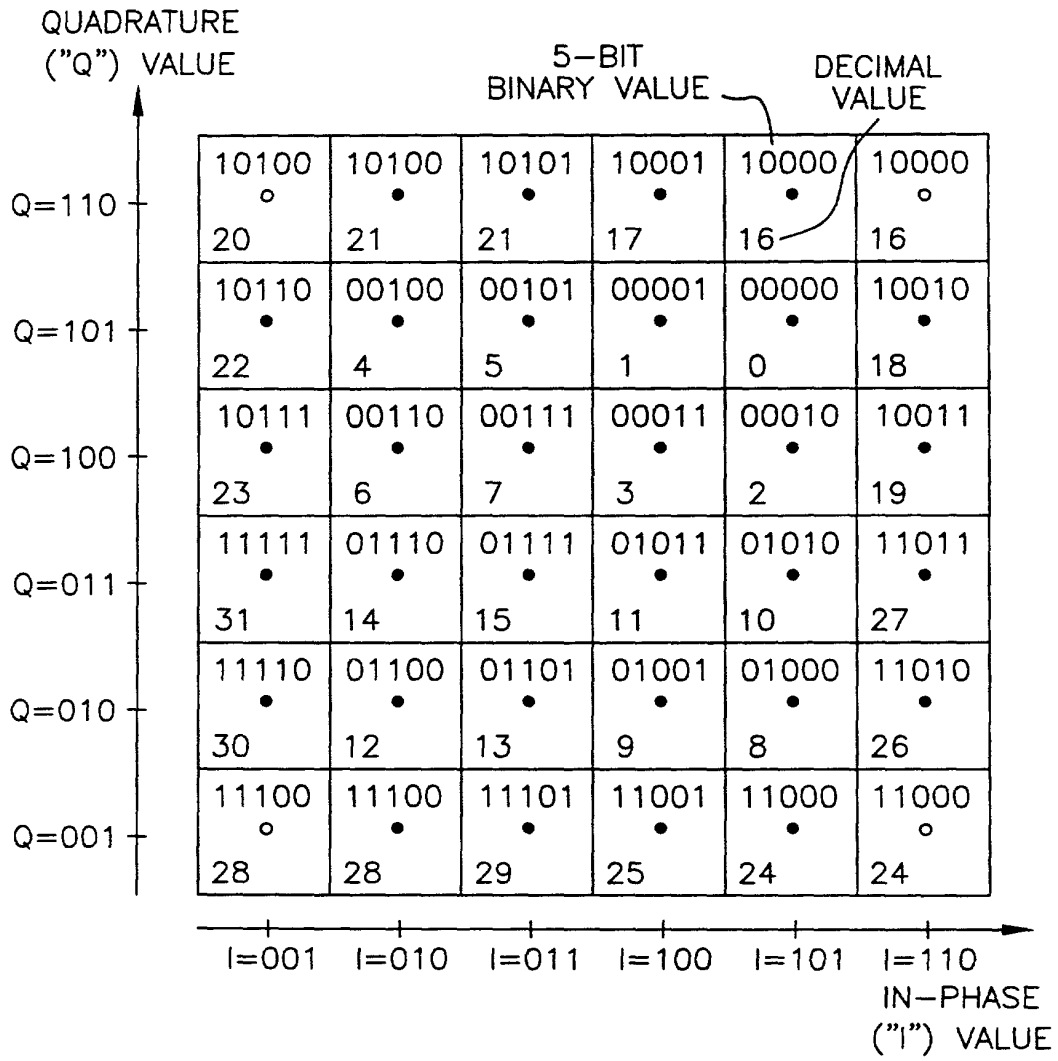

QUADRATURE
("Q") VALUE
5-BIT
BINARY VALUE
DECIMAL
VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE
("I") VALUE

FIG. 17

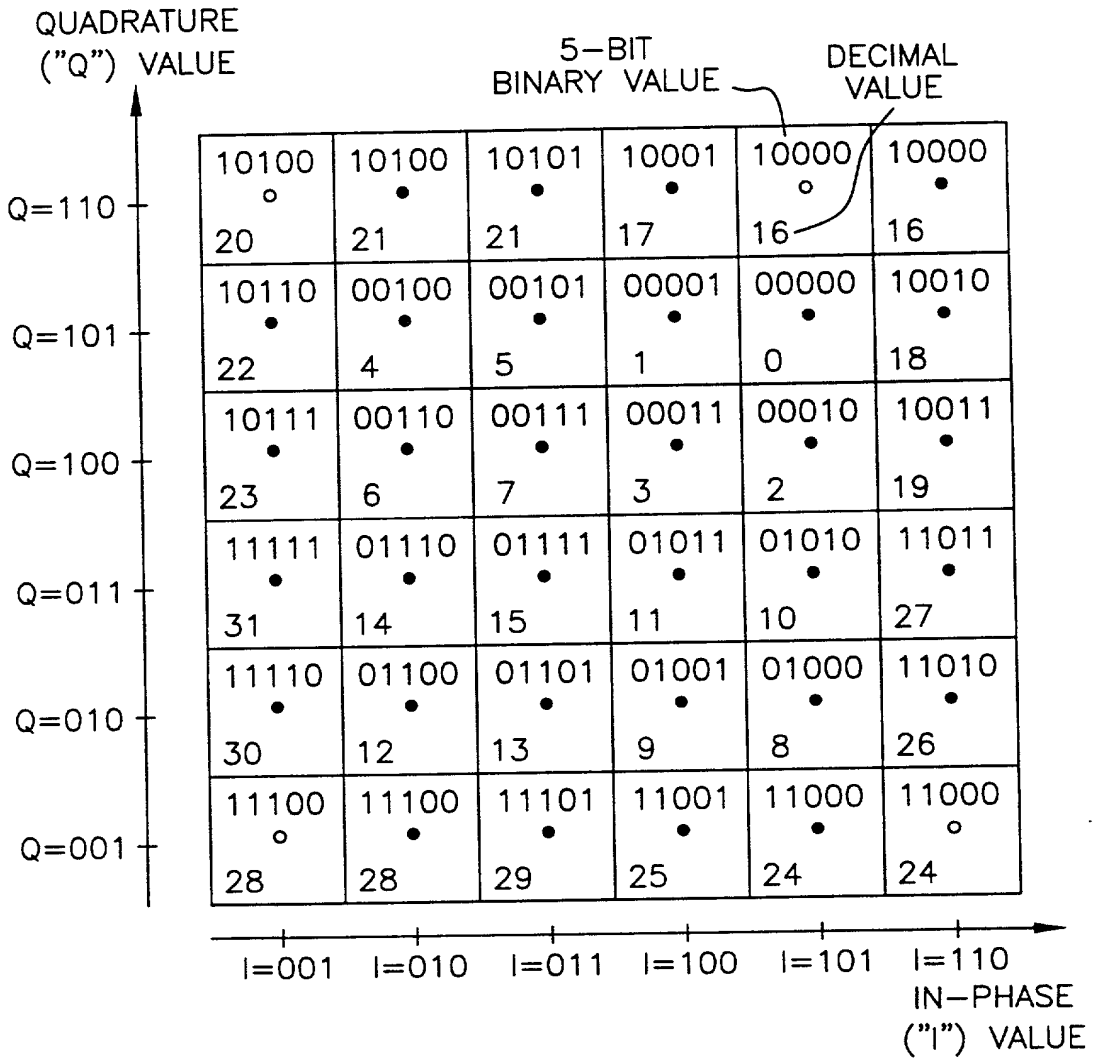

QUADRATURE ("Q") VALUE
5-BIT BINARY VALUE
DECIMAL VALUE
Q=110
Q=101
Q=100
Q=011
Q=010
Q=001
10100 20
10100 21
10101 21
10001 17
10000 16
10000 16
10110 22
00100 4
00101 5
00001 1
00000 0
10010 18
10111 23
00110 6
00111 7
00011 3
00010 2
10011 19
11111 31
01110 14
01111 15
01011 11
01010 10
11011 27
11110 30
01100 12
01101 13
01001 9
01000 8
11010 26
11100 28
11100 28
11101 29
11001 25
11000 24
11000 24
I=001
I=010
I=011
I=100
I=101
I=110
IN-PHASE ("I") VALUE

FIG. 18

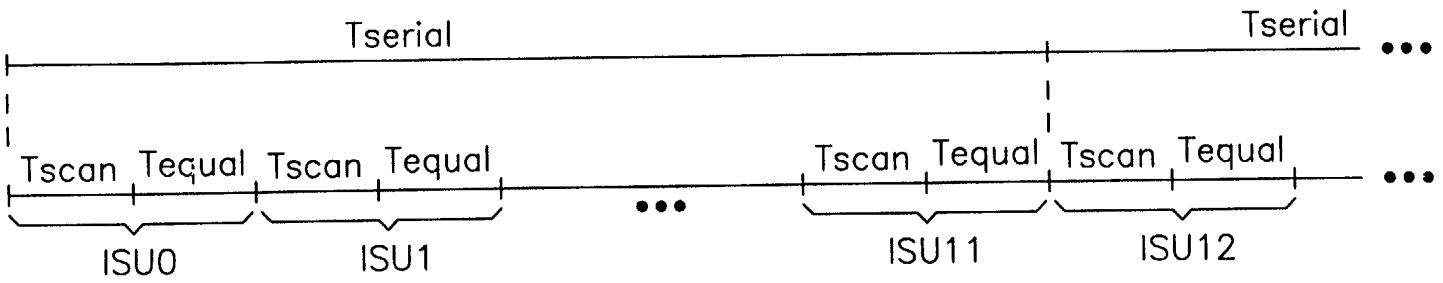

Tserial
Tserial
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
Tscan
Tequal
ISU0
ISU1
ISU11
ISU12

FIG. 19

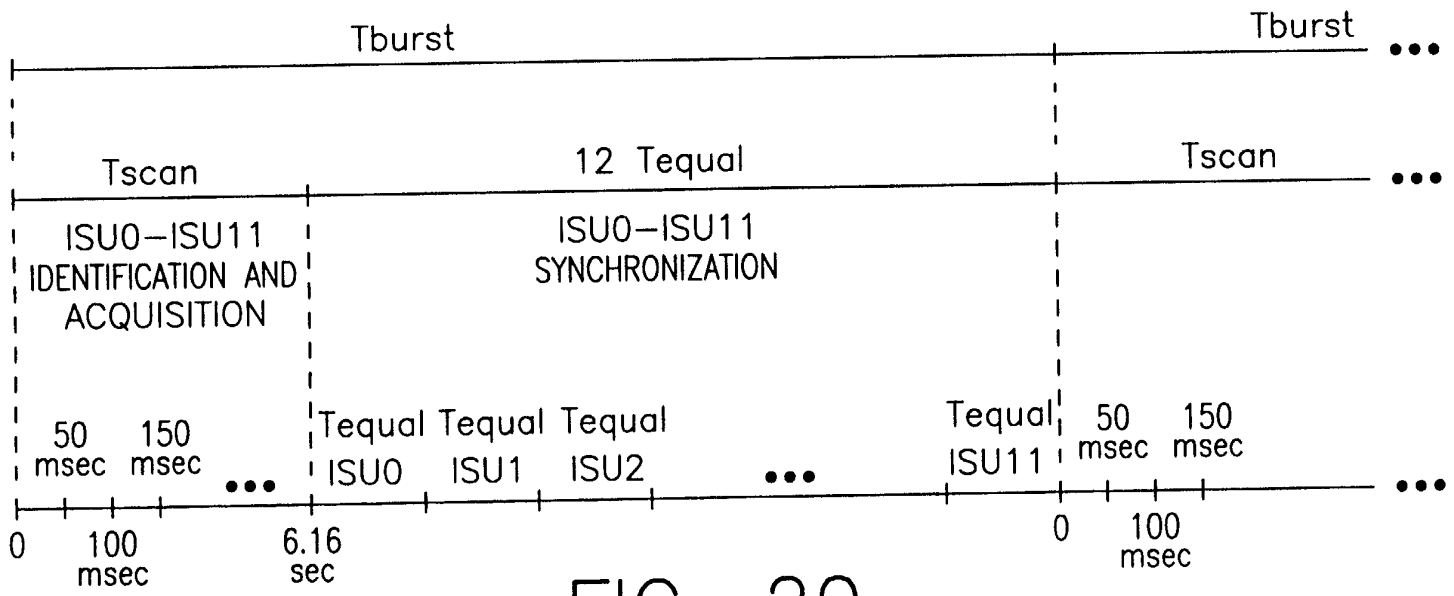

Tburst
Tburst
Tscan
12 Tequal
Tscan
ISU0–ISU11
IDENTIFICATION AND
ACQUISITION
ISU0–ISU11
SYNCHRONIZATION
50
msec
150
msec
Tequal
ISU0
Tequal
ISU1
Tequal
ISU2
Tequal
ISU11
50
msec
150
msec
0
100
msec
6.16
sec
0
100
msec

FIG. 20

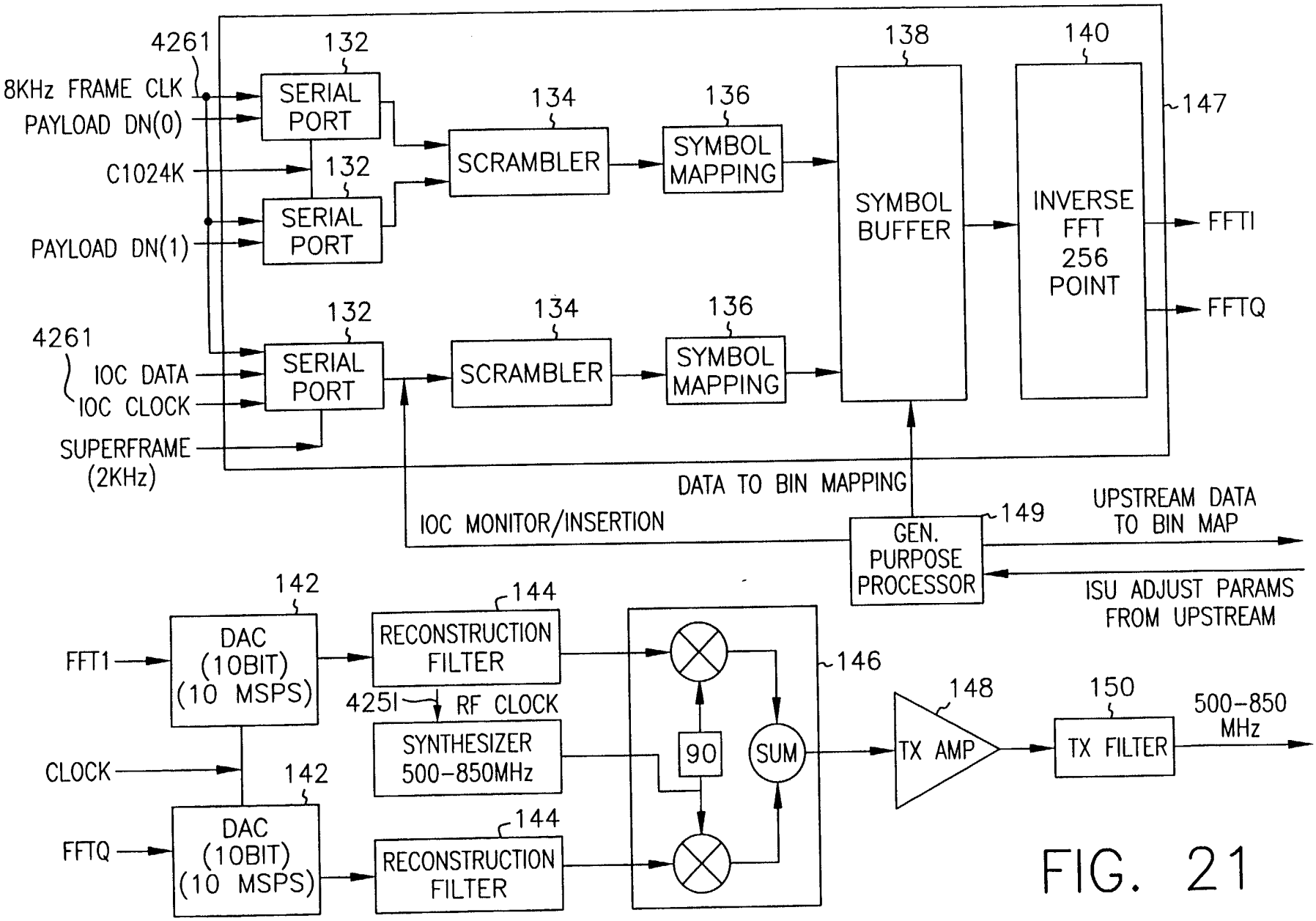

4261
132
138
140
8KHz FRAME CLK
PAYLOAD DN(0)
SERIAL PORT
134
136
SCRAMBLER
SYMBOL MAPPING
147
C1024K
132
SERIAL PORT
SYMBOL BUFFER
INVERSE FFT 256 POINT
FFTI
PAYLOAD DN(1)
FFTQ
4261
132
134
136
IOC DATA
IOC CLOCK
SERIAL PORT
SCRAMBLER
SYMBOL MAPPING
SUPERFRAME (2KHz)
DATA TO BIN MAPPING
IOC MONITOR/INSERTION
149
GEN. PURPOSE PROCESSOR
UPSTREAM DATA TO BIN MAP
ISU ADJUST PARAMS FROM UPSTREAM
142
144
FFT1
DAC (10BIT) (10 MSPS)
RECONSTRUCTION FILTER
146
4251
RF CLOCK
SYNTHESIZER 500-850MHz
90
SUM
148
150
500-850 MHz
TX AMP
TX FILTER
CLOCK
142
144
FFTQ
DAC (10BIT) (10 MSPS)
RECONSTRUCTION FILTER

FIG. 21

SOFTSCAN

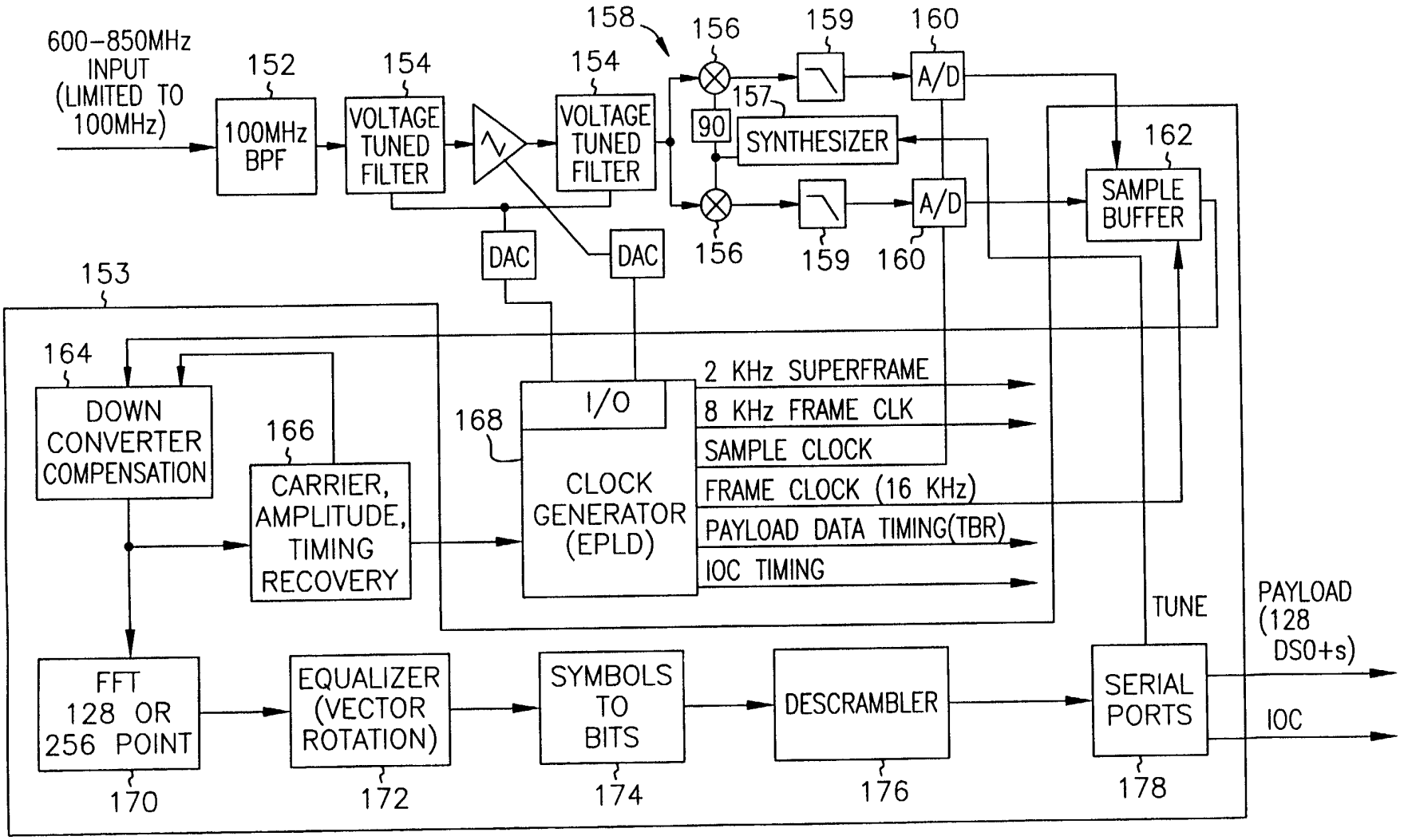


FIG. 22

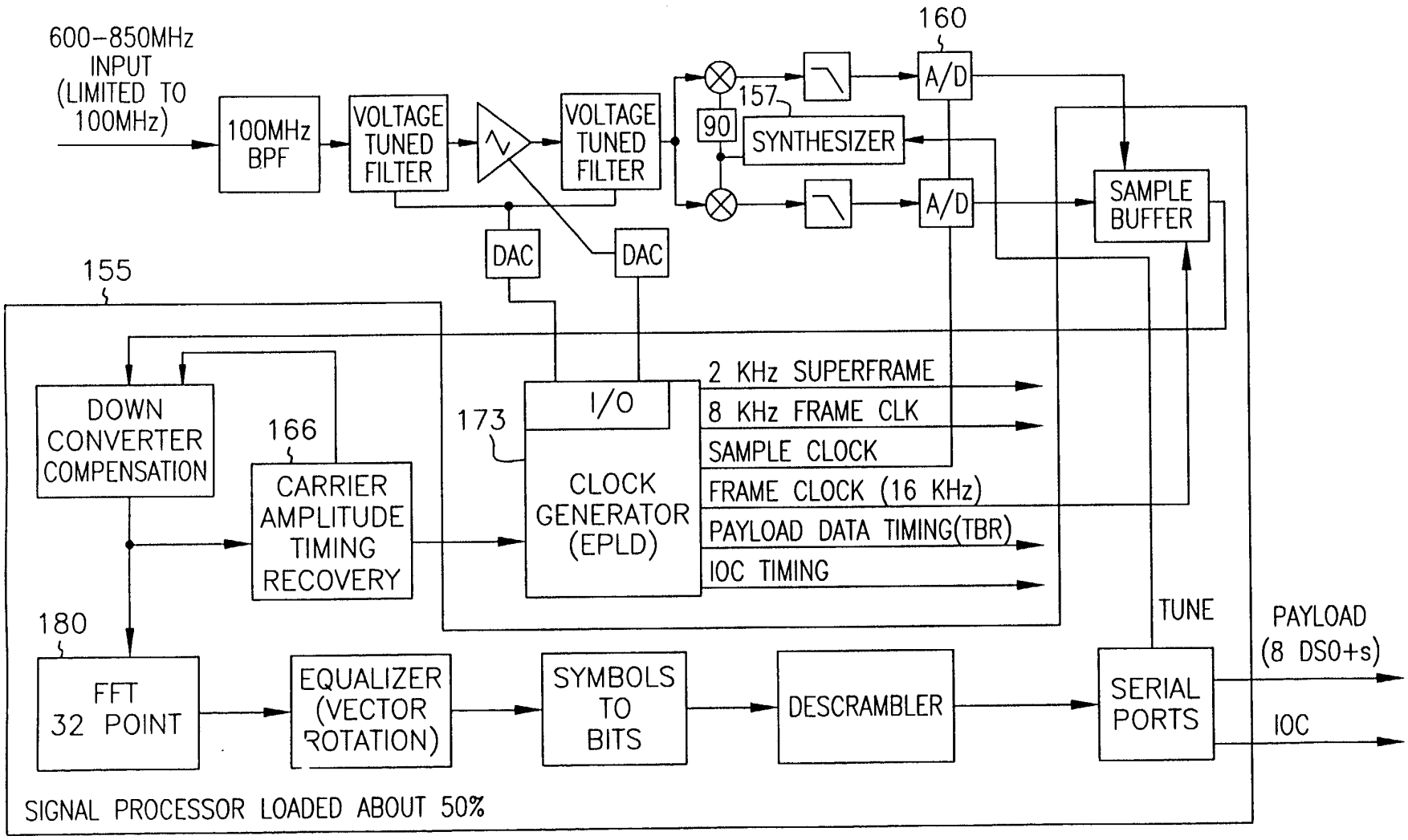

600–850MHz
INPUT
(LIMITED TO
100MHz)
100MHz
BPF
VOLTAGE
TUNED
FILTER
VOLTAGE
TUNED
FILTER
160
A/D
157
90
SYNTHESIZER
A/D
SAMPLE
BUFFER
DAC
DAC
155
DOWN
CONVERTER
COMPENSATION
166
CARRIER
AMPLITUDE
TIMING
RECOVERY
173
I/O
CLOCK
GENERATOR
(EPLD)
2 KHz SUPERFRAME
8 KHz FRAME CLK
SAMPLE CLOCK
FRAME CLOCK (16 KHz)
PAYLOAD DATA TIMING(TBR)
IOC TIMING
TUNE
PAYLOAD
(8 DS0+s)
180
FFT
32 POINT
EQUALIZER
(VECTOR
ROTATION)
SYMBOLS
TO
BITS
DESCRAMBLER
SERIAL
PORTS
IOC
SIGNAL PROCESSOR LOADED ABOUT 50%

FIG. 23

DRAFT PROPOSED

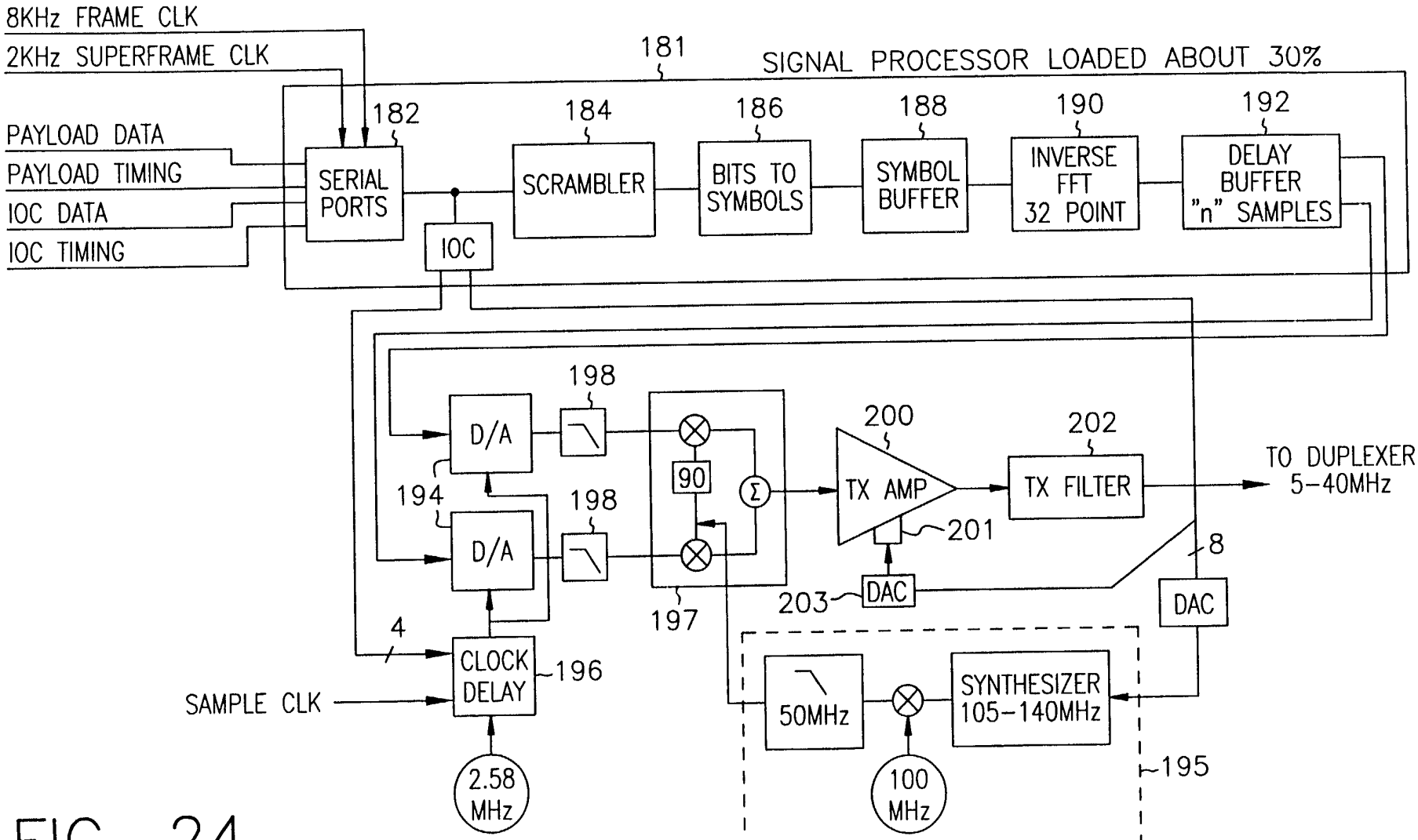


FIG. 24

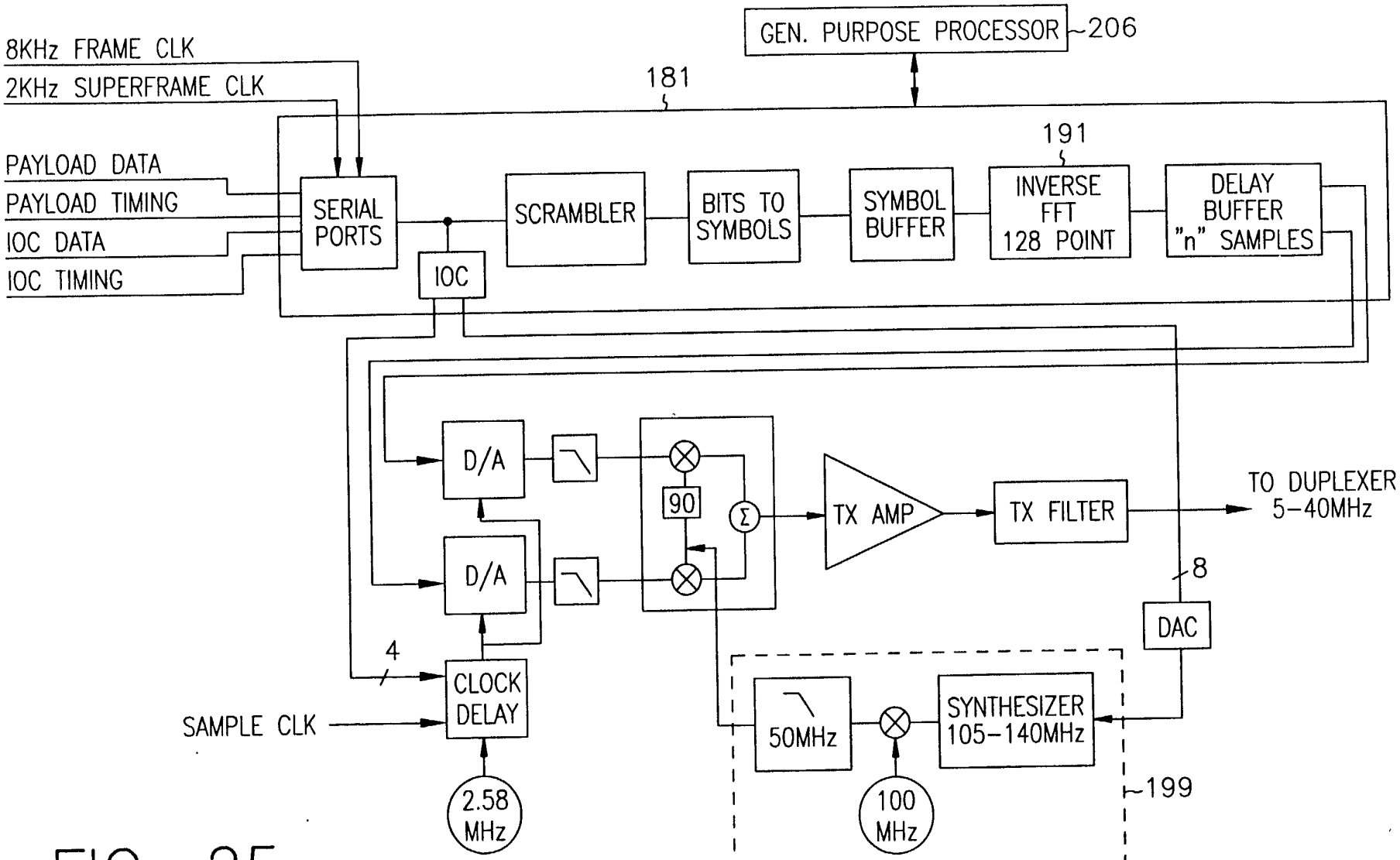

GEN. PURPOSE PROCESSOR
206
181
191
8KHz FRAME CLK
2KHz SUPERFRAME CLK
PAYLOAD DATA
PAYLOAD TIMING
IOC DATA
IOC TIMING
SERIAL PORTS
IOC
SCRAMBLER
BITS TO SYMBOLS
SYMBOL BUFFER
INVERSE FFT 128 POINT
DELAY BUFFER "n" SAMPLES
D/A
D/A
90
Σ
TX AMP
TX FILTER
TO DUPLEXER 5-40MHz
8
DAC
4
CLOCK DELAY
SAMPLE CLK
2.58 MHz
50MHz
100 MHz
SYNTHESIZER 105-140MHz
199

FIG. 25

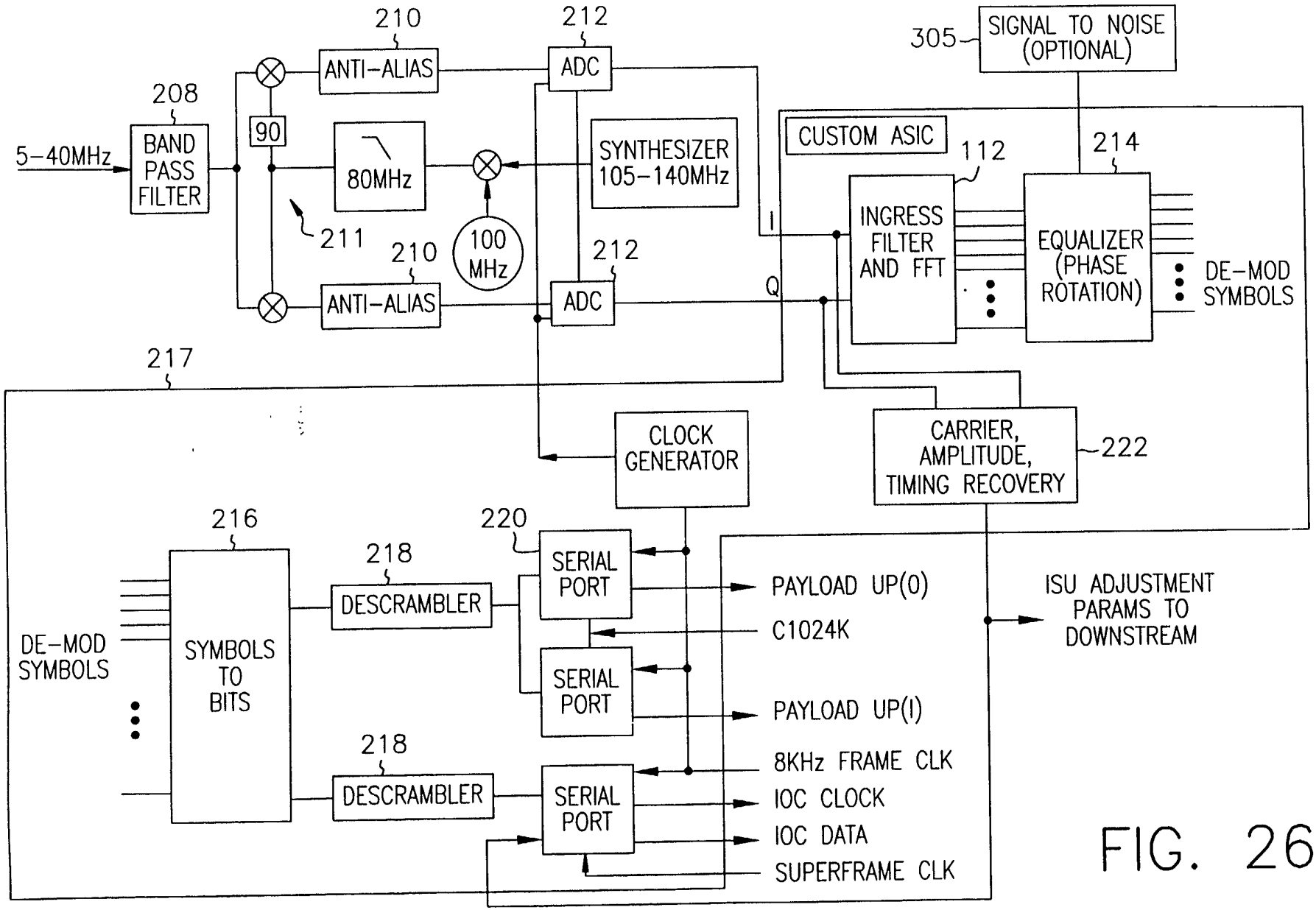

210
212
305
SIGNAL TO NOISE (OPTIONAL)
208
ANTI-ALIAS
ADC
5-40MHz
BAND PASS FILTER
90
80MHz
SYNTHESIZER 105-140MHz
CUSTOM ASIC
112
214
211
100 MHz
I
INGRESS FILTER AND FFT
EQUALIZER (PHASE ROTATION)
DE-MOD SYMBOLS
210
212
ANTI-ALIAS
ADC
Q
217
CLOCK GENERATOR
CARRIER, AMPLITUDE, TIMING RECOVERY
222
216
220
218
SERIAL PORT
PAYLOAD UP(0)
DESCRAMBLER
C1024K
DE-MOD SYMBOLS
SYMBOLS TO BITS
SERIAL PORT
PAYLOAD UP(I)
218
8KHz FRAME CLK
DESCRAMBLER
SERIAL PORT
IOC CLOCK
IOC DATA
SUPERFRAME CLK
ISU ADJUSTMENT PARAMS TO DOWNSTREAM

FIG. 26

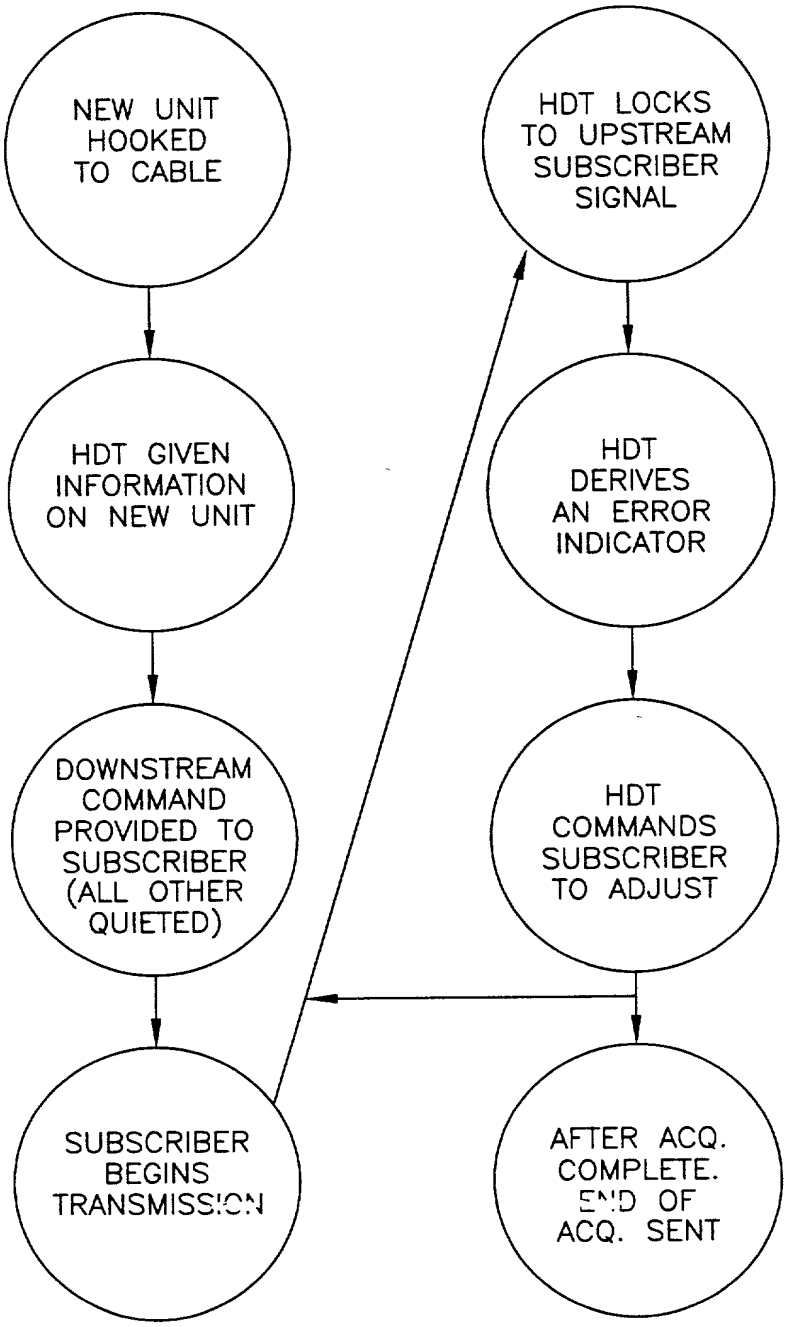

NEW UNIT HOOKED TO CABLE
HDT GIVEN INFORMATION ON NEW UNIT
DOWNSTREAM COMMAND PROVIDED TO SUBSCRIBER (ALL OTHER QUIETED)
SUBSCRIBER BEGINS TRANSMISSION
HDT LOCKS TO UPSTREAM SUBSCRIBER SIGNAL
HDT DERIVES AN ERROR INDICATOR
HDT COMMANDS SUBSCRIBER TO ADJUST
AFTER ACQ. COMPLETE. END OF ACQ. SENT

FIG. 27

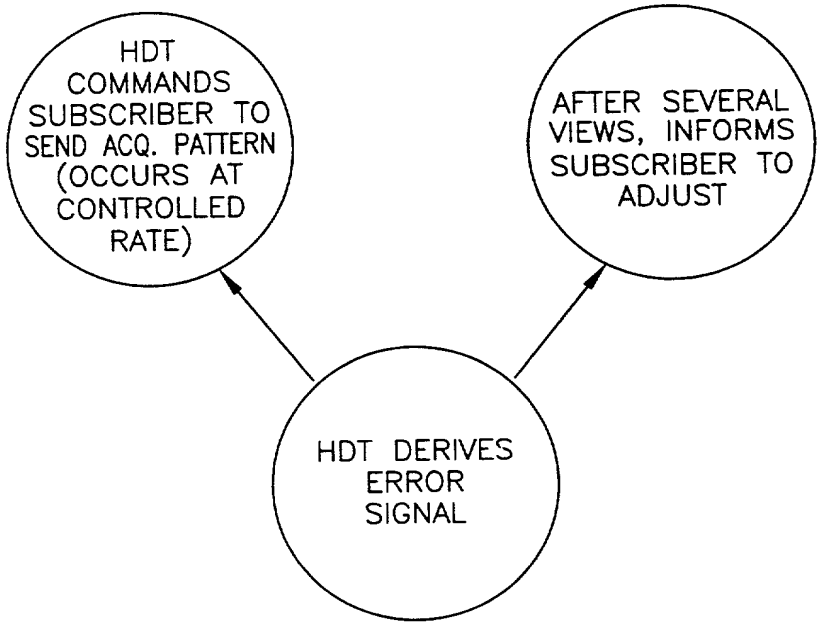

HDT COMMANDS SUBSCRIBER TO SEND ACQ. PATTERN (OCCURS AT CONTROLLED RATE)
AFTER SEVERAL VIEWS, INFORMS SUBSCRIBER TO ADJUST
HDT DERIVES ERROR SIGNAL

FIG. 28

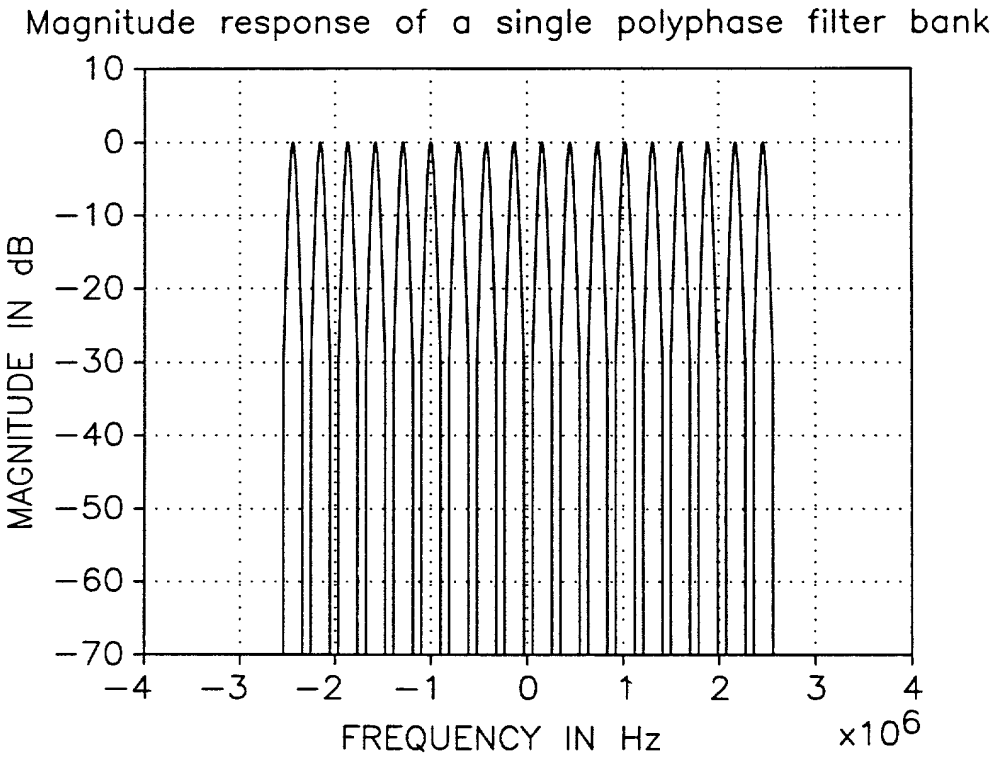

Magnitude response of a single polyphase filter bank
10
0
−10
−20
−30
−40
−50
−60
−70
MAGNITUDE IN dB
−4
−3
−2
−1
0
1
2
3
4
FREQUENCY IN Hz
x10^6

FIG. 29

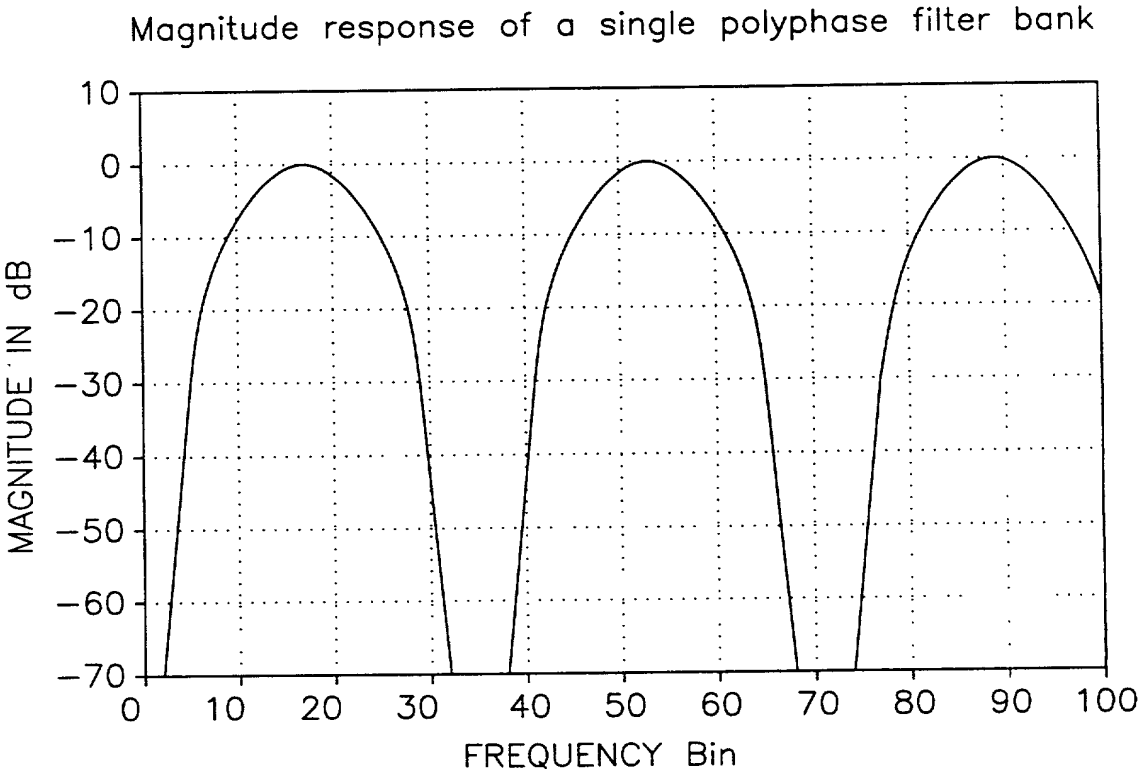

Magnitude response of a single polyphase filter bank
MAGNITUDE IN dB
10
0
−10
−20
−30
−40
−50
−60
−70
0
10
20
30
40
50
60
70
80
90
100
FREQUENCY Bin

FIG. 30

Patent Search

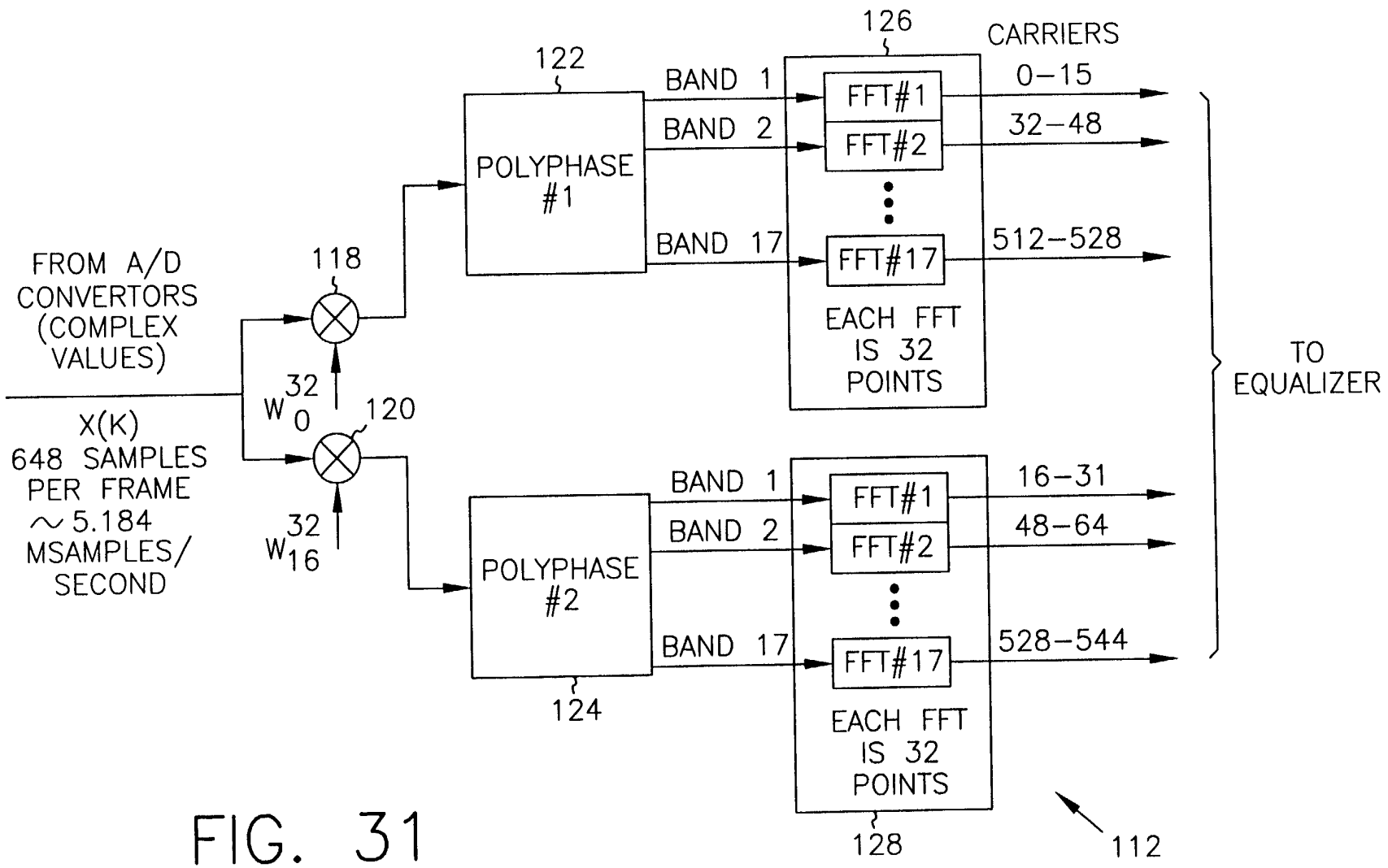


FIG. 31

20170 ES2 EP0

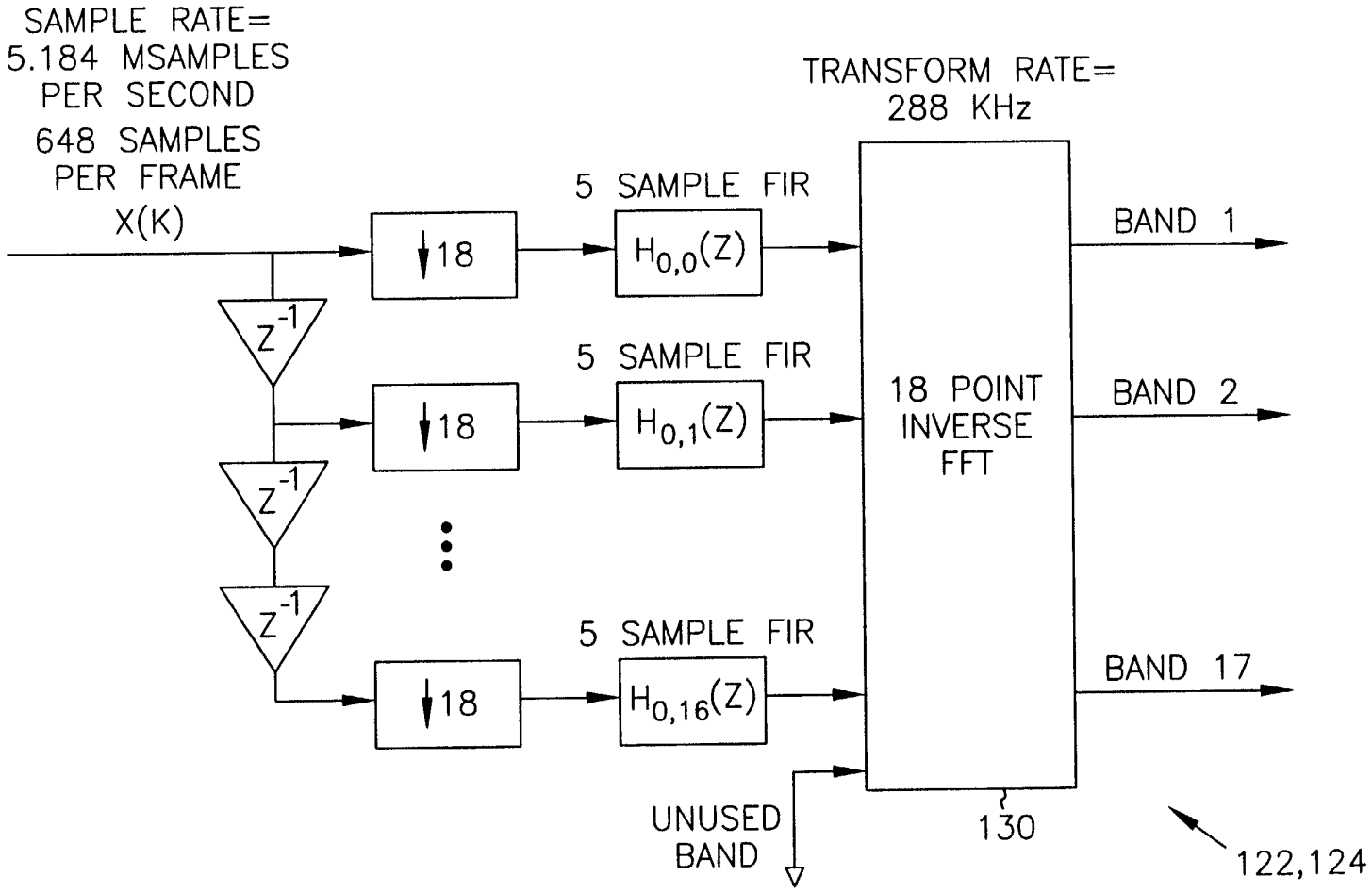
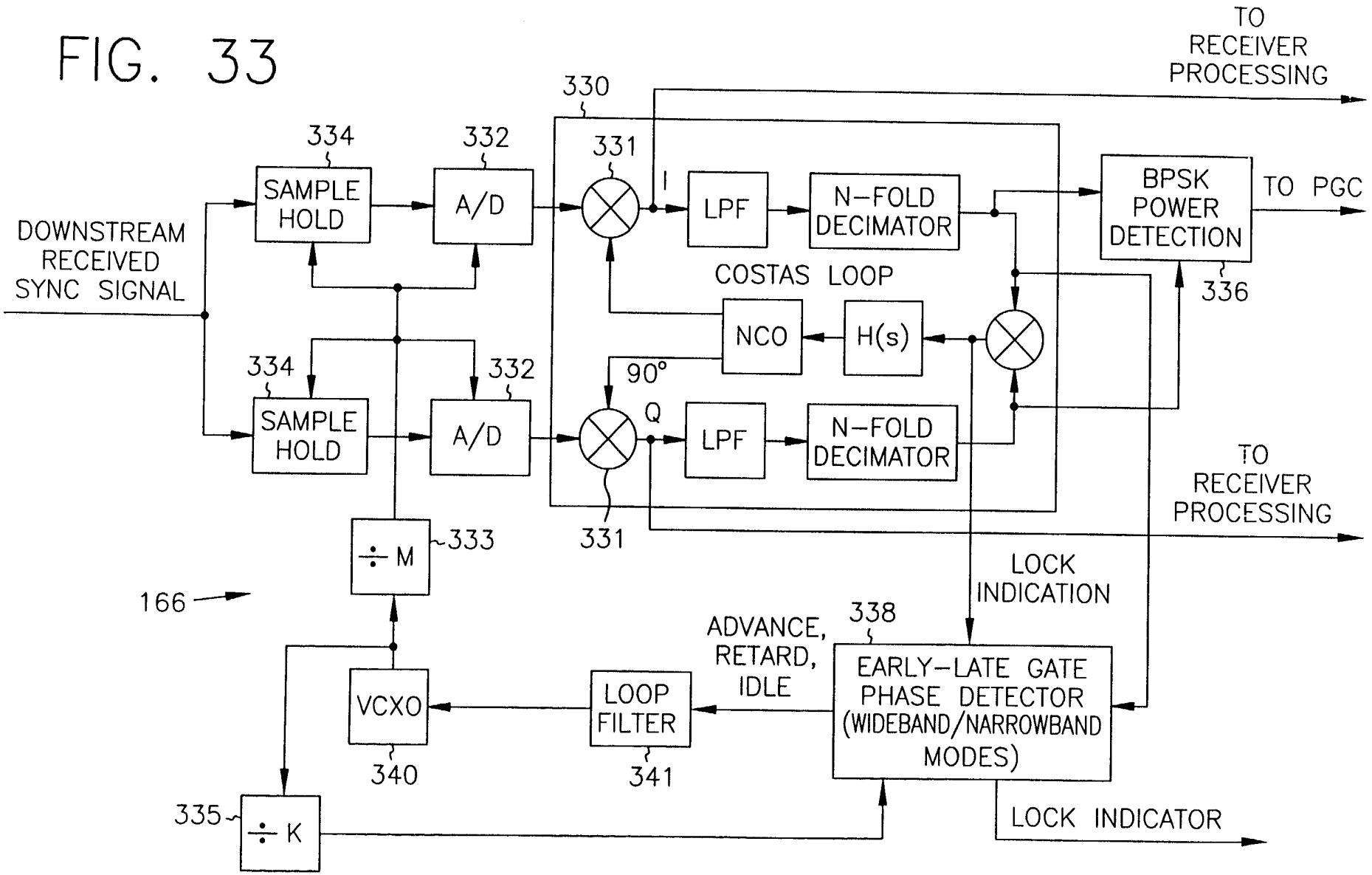


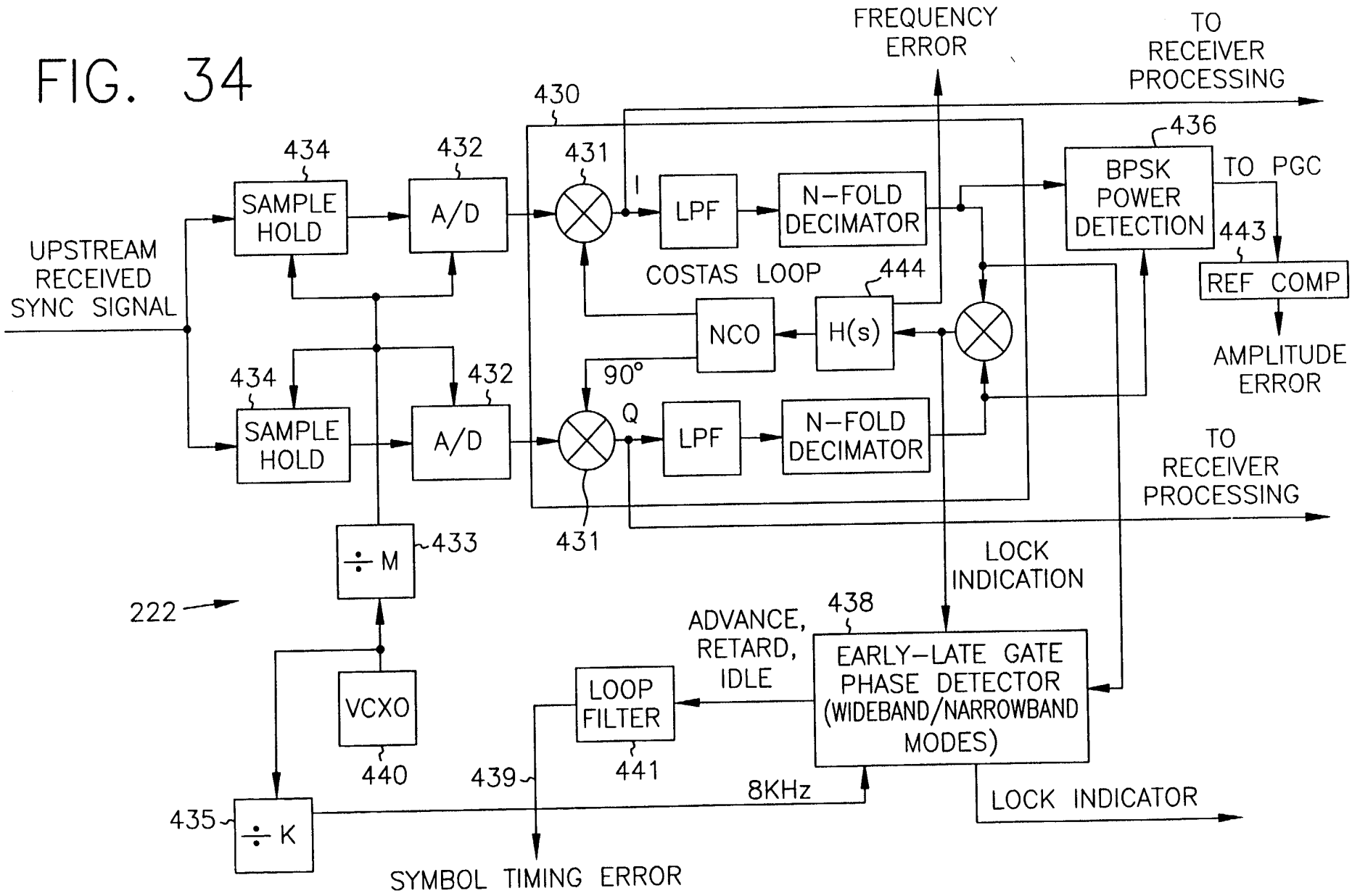
FIG. 32

FIG. 33


TO RECEIVER PROCESSING
330
334
332
331
SAMPLE HOLD
A/D
I
LPF
N-FOLD DECIMATOR
BPSK POWER DETECTION
TO PGC
DOWNSTREAM RECEIVED SYNC SIGNAL
COSTAS LOOP
NCO
H(s)
336
334
332
90°
SAMPLE HOLD
A/D
Q
LPF
N-FOLD DECIMATOR
TO RECEIVER PROCESSING
÷ M
333
331
LOCK INDICATION
166
338
ADVANCE, RETARD, IDLE
EARLY-LATE GATE PHASE DETECTOR (WIDEBAND/NARROWBAND MODES)
VCXO
LOOP FILTER
340
341
335
÷ K
LOCK INDICATOR

Patent Search

FIG. 34



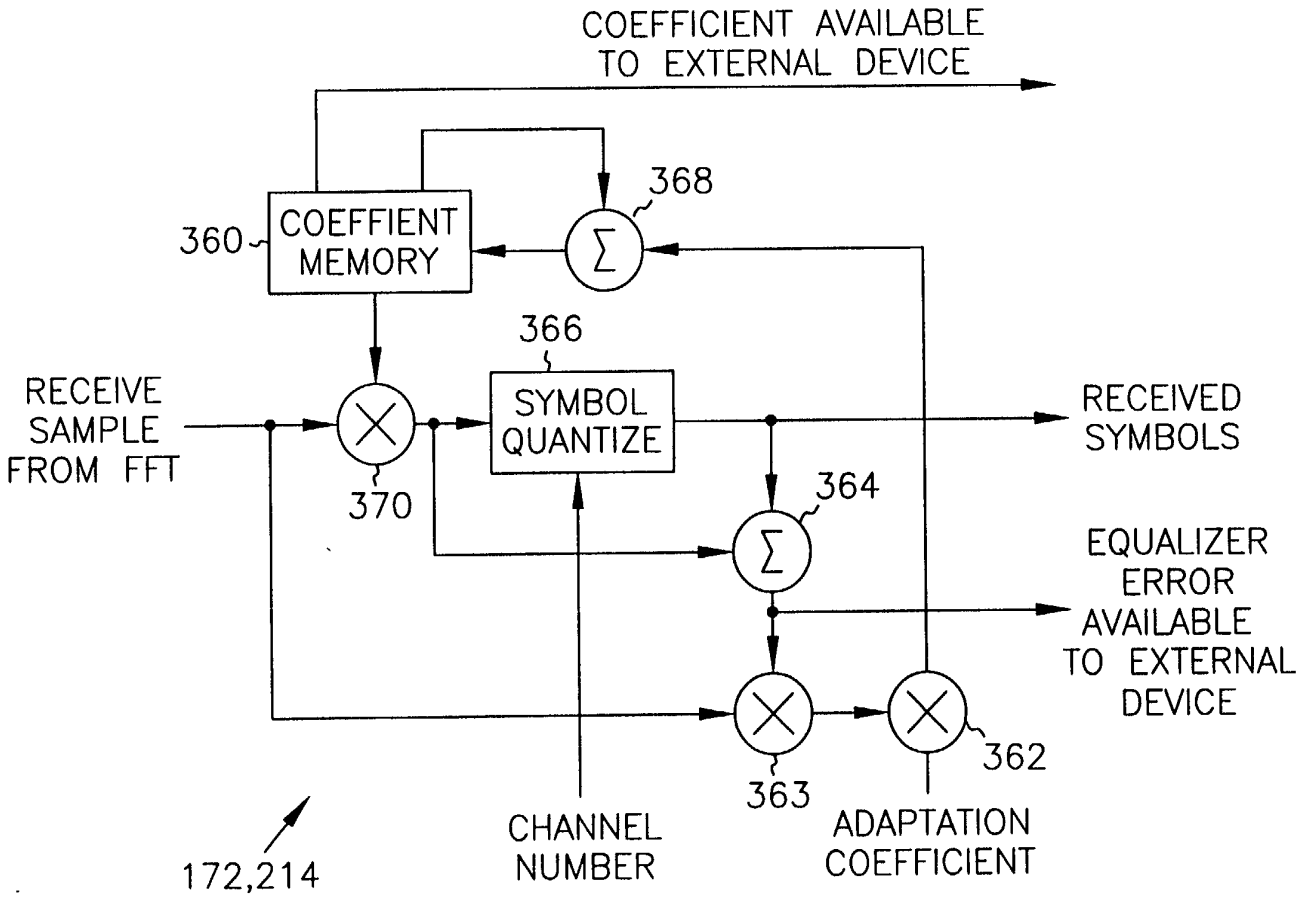

COEFFICIENT AVAILABLE
TO EXTERNAL DEVICE
368
360
COEFFIENT
MEMORY
366
RECEIVE
SAMPLE
FROM FFT
SYMBOL
QUANTIZE
RECEIVED
SYMBOLS
370
364
EQUALIZER
ERROR
AVAILABLE
TO EXTERNAL
DEVICE
362
363
172,214
CHANNEL
NUMBER
ADAPTATION
COEFFICIENT

FIG. 35

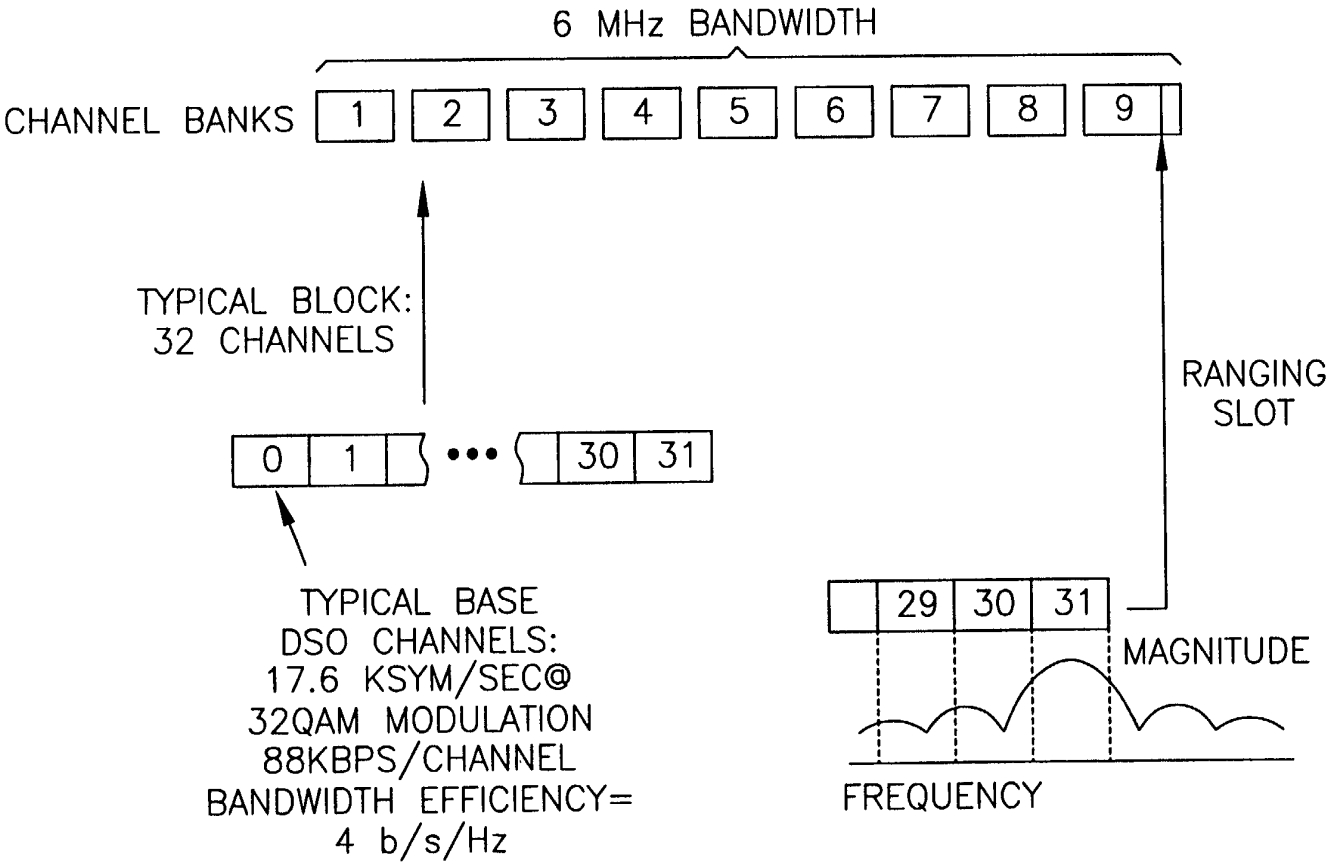

6 MHz BANDWIDTH
CHANNEL BANKS
1
2
3
4
5
6
7
8
9
TYPICAL BLOCK:
32 CHANNELS
0
1
30
31
RANGING
SLOT
TYPICAL BASE
DSO CHANNELS:
17.6 KSYM/SEC@
32QAM MODULATION
88KBPS/CHANNEL
BANDWIDTH EFFICIENCY=
4 b/s/Hz
29
30
31
MAGNITUDE
FREQUENCY

FIG. 36

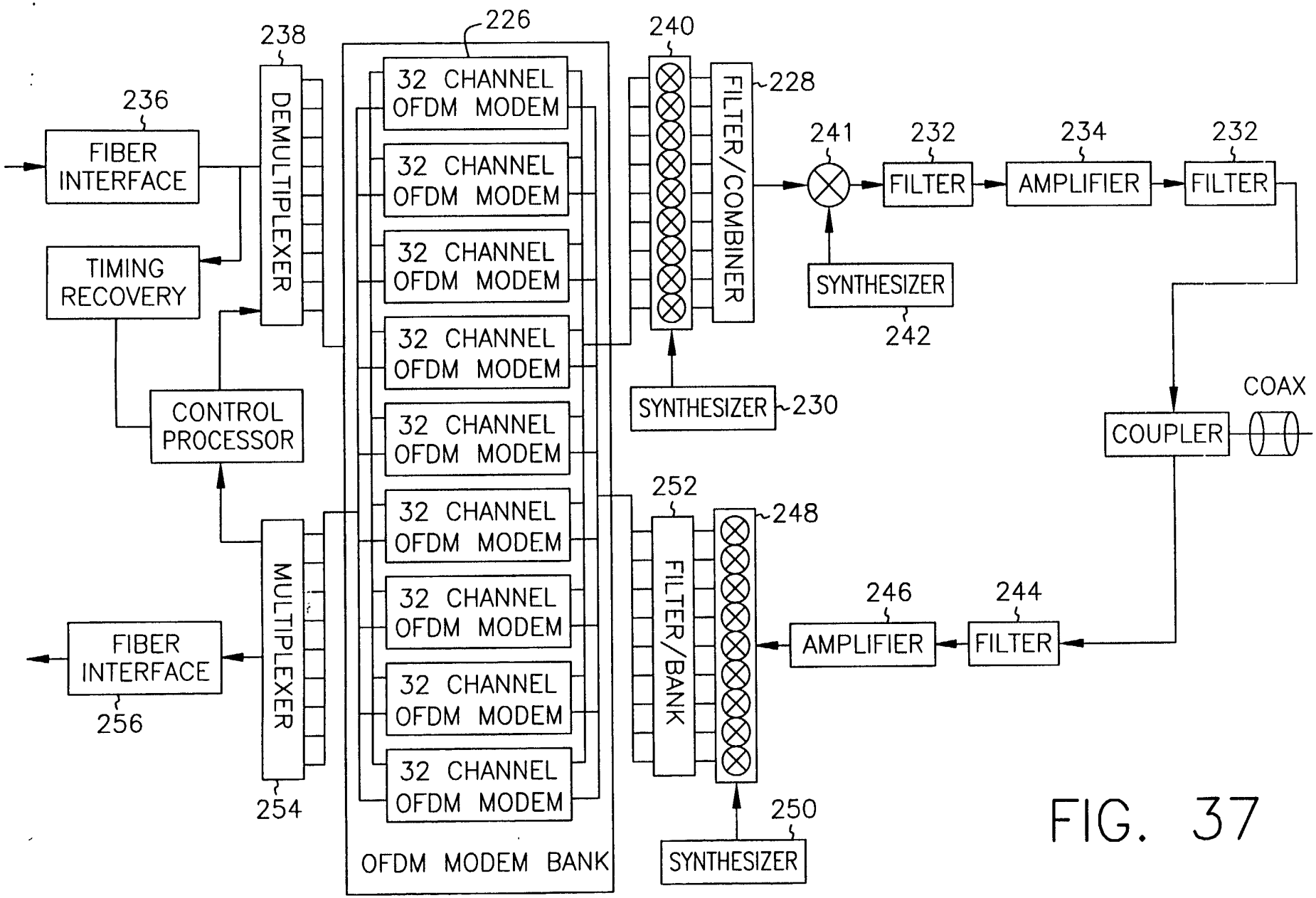

226
238
240
236
32 CHANNEL OFDM MODEM
DEMULTIPLEXER
FILTER/COMBINER
228
FIBER INTERFACE
241
232
234
232
FILTER
AMPLIFIER
FILTER
TIMING RECOVERY
SYNTHESIZER
242
COAX
CONTROL PROCESSOR
SYNTHESIZER
230
COUPLER
252
248
MULTIPLEXER
FILTER/BANK
246
244
AMPLIFIER
FILTER
FIBER INTERFACE
256
254
250
SYNTHESIZER
OFDM MODEM BANK

FIG. 37

Patent Application

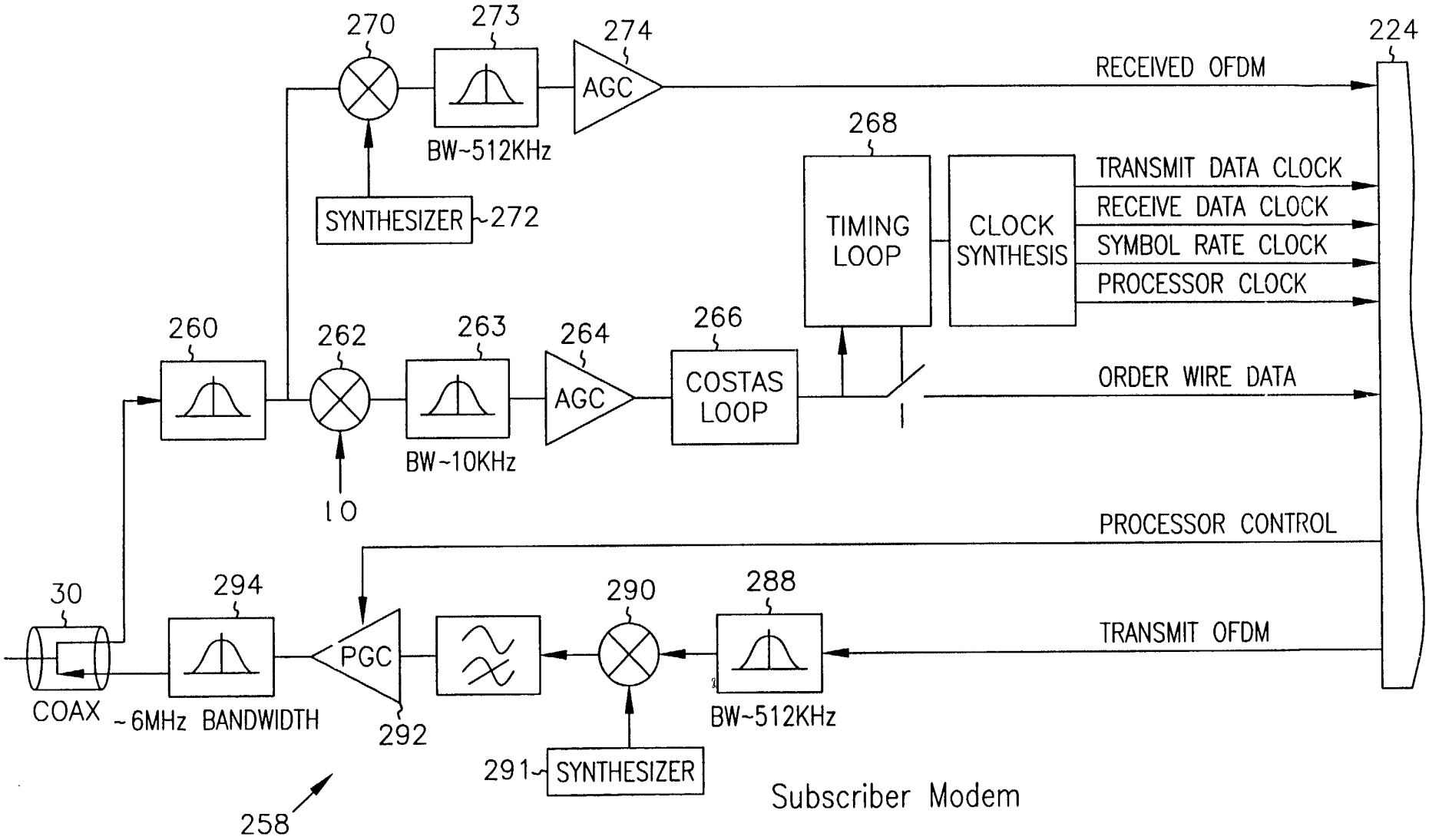


FIG. 38

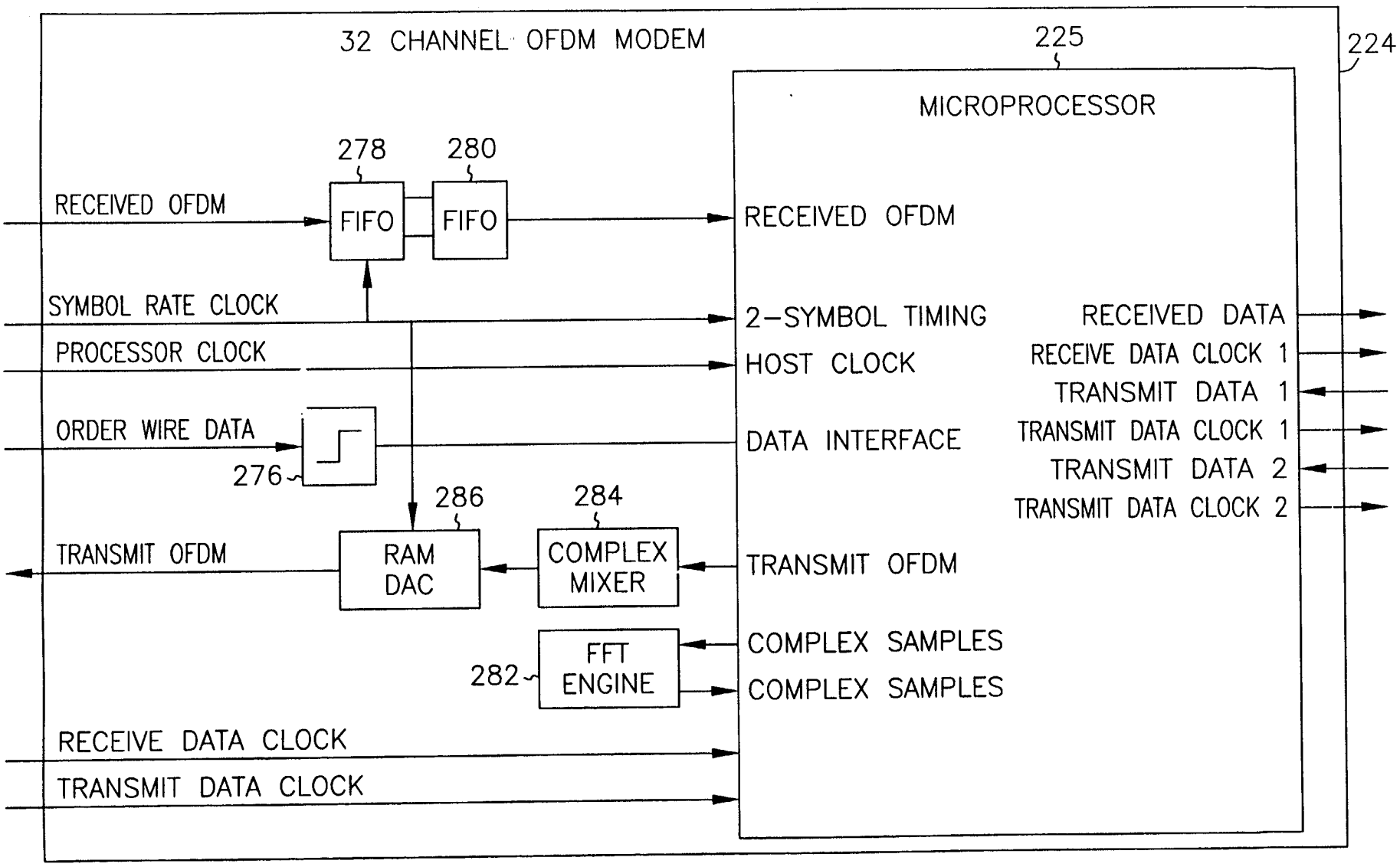

32 CHANNEL OFDM MODEM
225
224
MICROPROCESSOR
278
280
RECEIVED OFDM
FIFO
FIFO
RECEIVED OFDM
SYMBOL RATE CLOCK
2-SYMBOL TIMING
RECEIVED DATA
PROCESSOR CLOCK
HOST CLOCK
RECEIVE DATA CLOCK 1
TRANSMIT DATA 1
ORDER WIRE DATA
DATA INTERFACE
TRANSMIT DATA CLOCK 1
TRANSMIT DATA 2
276
TRANSMIT DATA CLOCK 2
286
284
TRANSMIT OFDM
RAM DAC
COMPLEX MIXER
TRANSMIT OFDM
COMPLEX SAMPLES
FFT ENGINE
282
COMPLEX SAMPLES
RECEIVE DATA CLOCK
TRANSMIT DATA CLOCK

FIG. 39

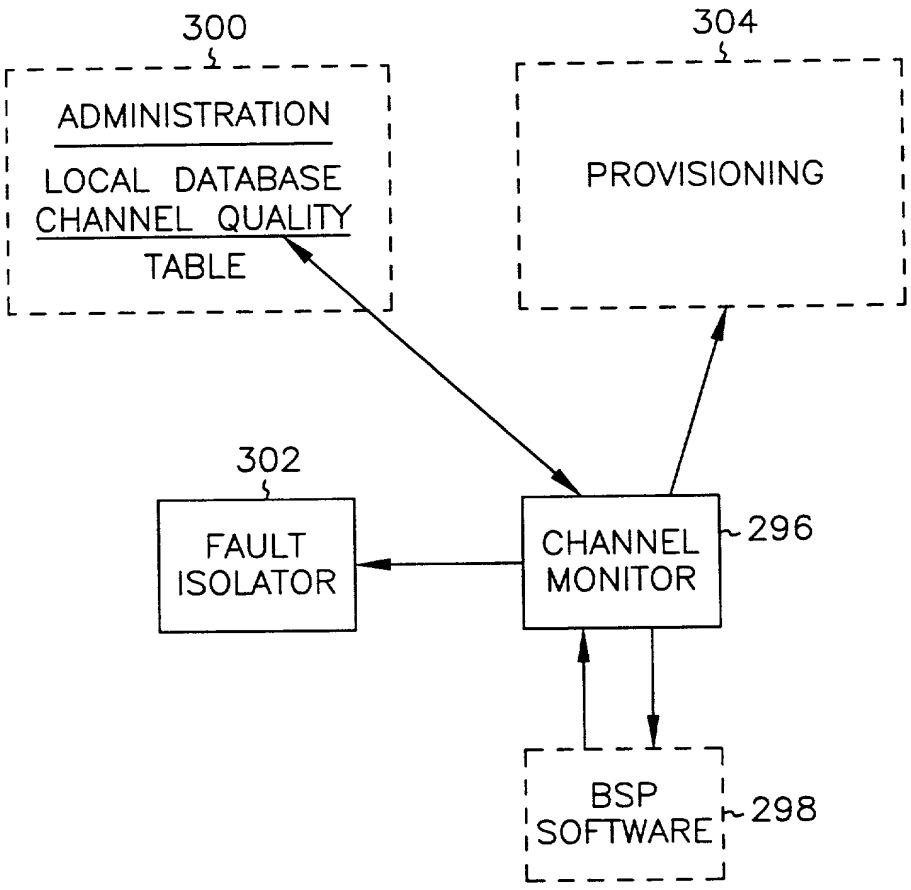

300
ADMINISTRATION
LOCAL DATABASE
CHANNEL QUALITY
TABLE
304
PROVISIONING
302
FAULT
ISOLATOR
CHANNEL
MONITOR
296
BSP
SOFTWARE
298

FIG. 40

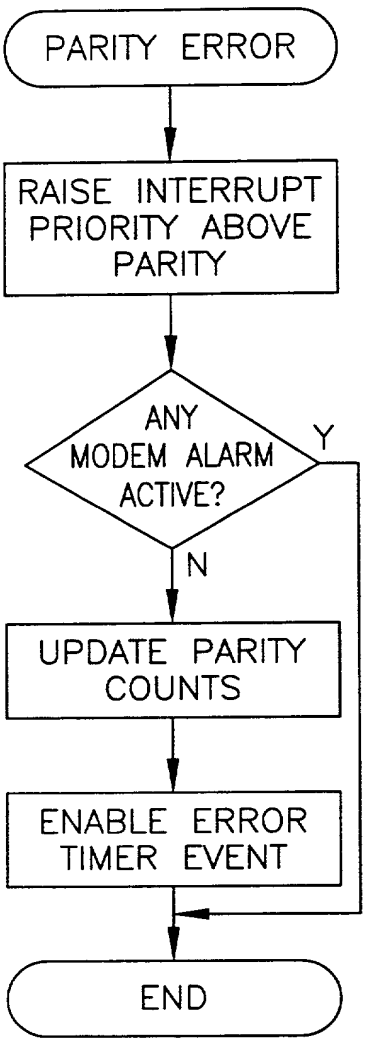


FIG. 41

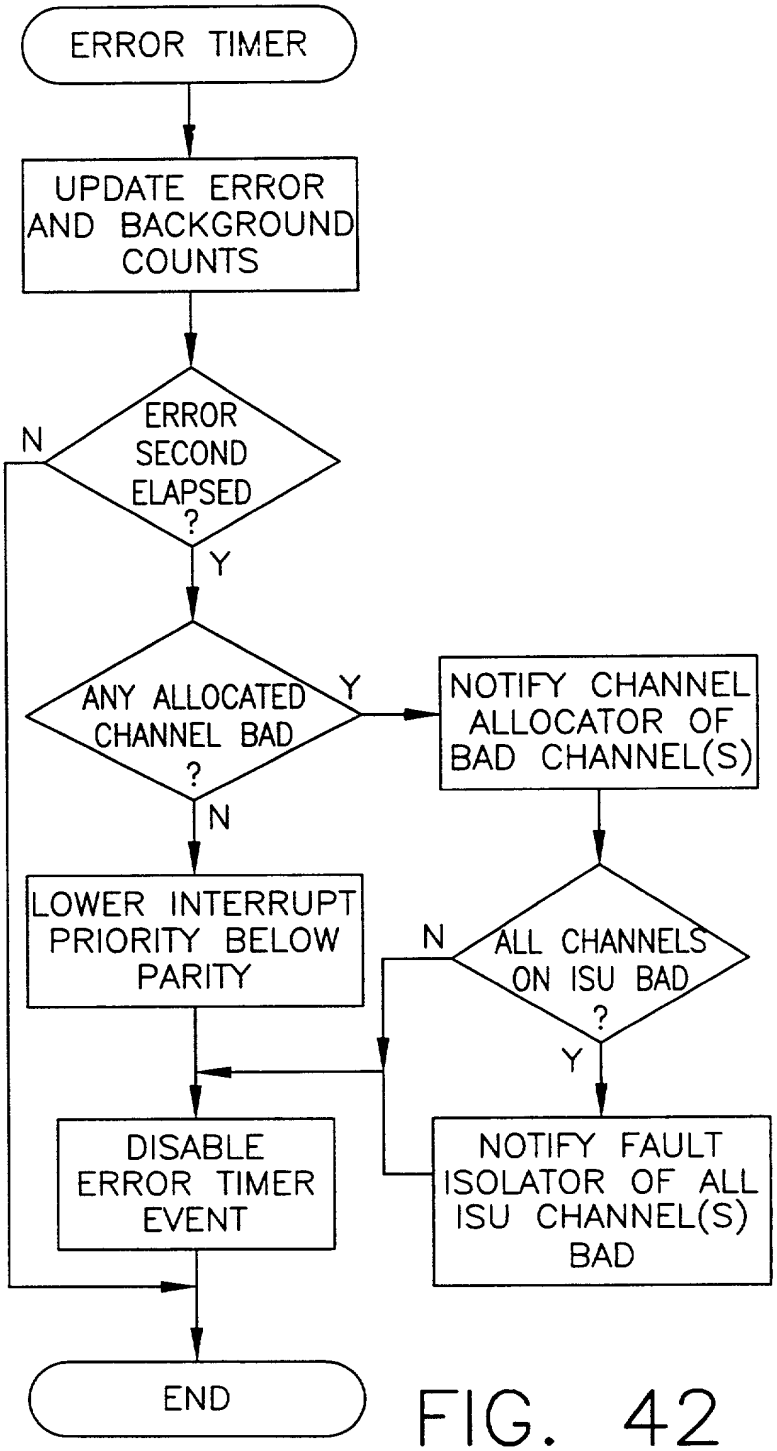


FIG. 42

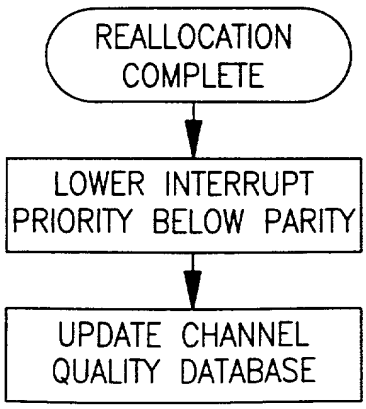
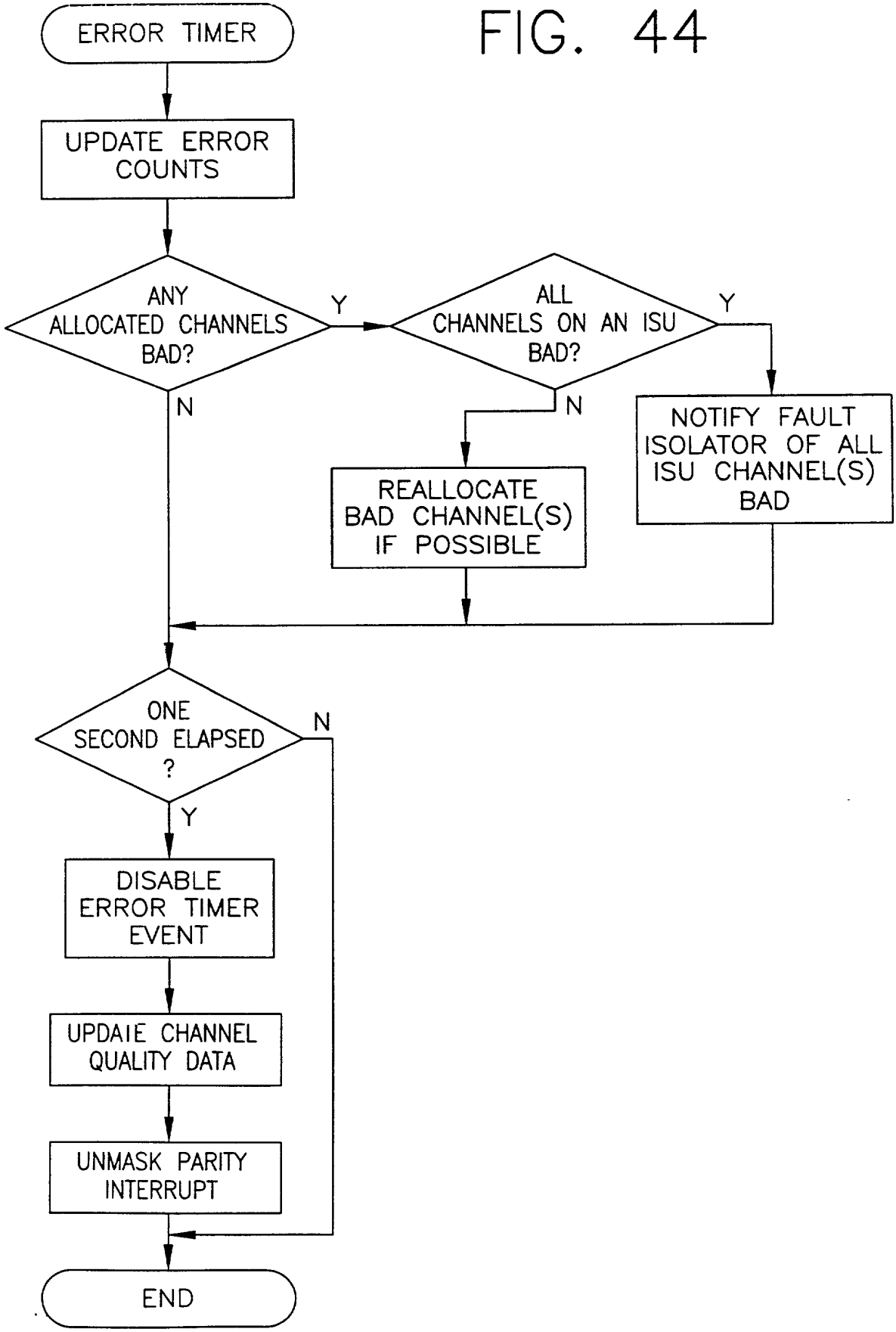


FIG. 43

FIG. 44


ERROR TIMER
UPDATE ERROR COUNTS
ANY ALLOCATED CHANNELS BAD?
Y
ALL CHANNELS ON AN ISU BAD?
Y
N
N
NOTIFY FAULT ISOLATOR OF ALL ISU CHANNEL(S) BAD
REALLOCATE BAD CHANNEL(S) IF POSSIBLE
ONE SECOND ELAPSED ?
N
Y
DISABLE ERROR TIMER EVENT
UPDAIE CHANNEL QUALITY DATA
UNMASK PARITY INTERRUPT
END

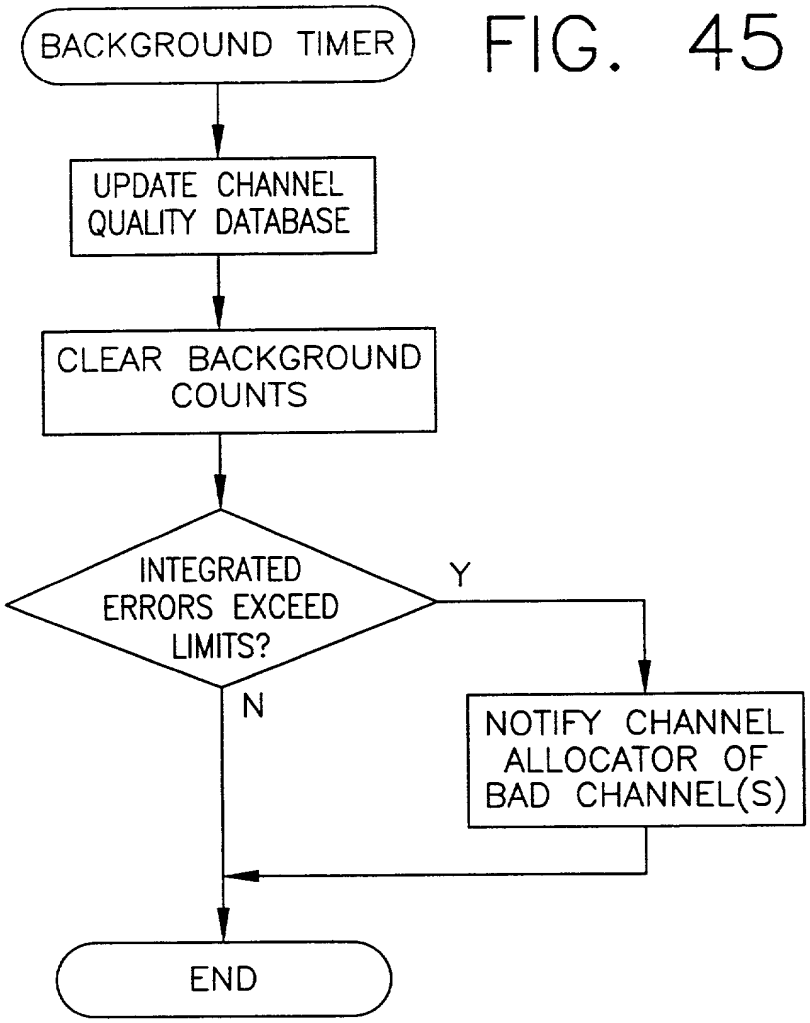

BACKGROUND TIMER
UPDATE CHANNEL QUALITY DATABASE
CLEAR BACKGROUND COUNTS
INTEGRATED ERRORS EXCEED LIMITS?
Y
N
NOTIFY CHANNEL ALLOCATOR OF BAD CHANNEL(S)
END

FIG. 45

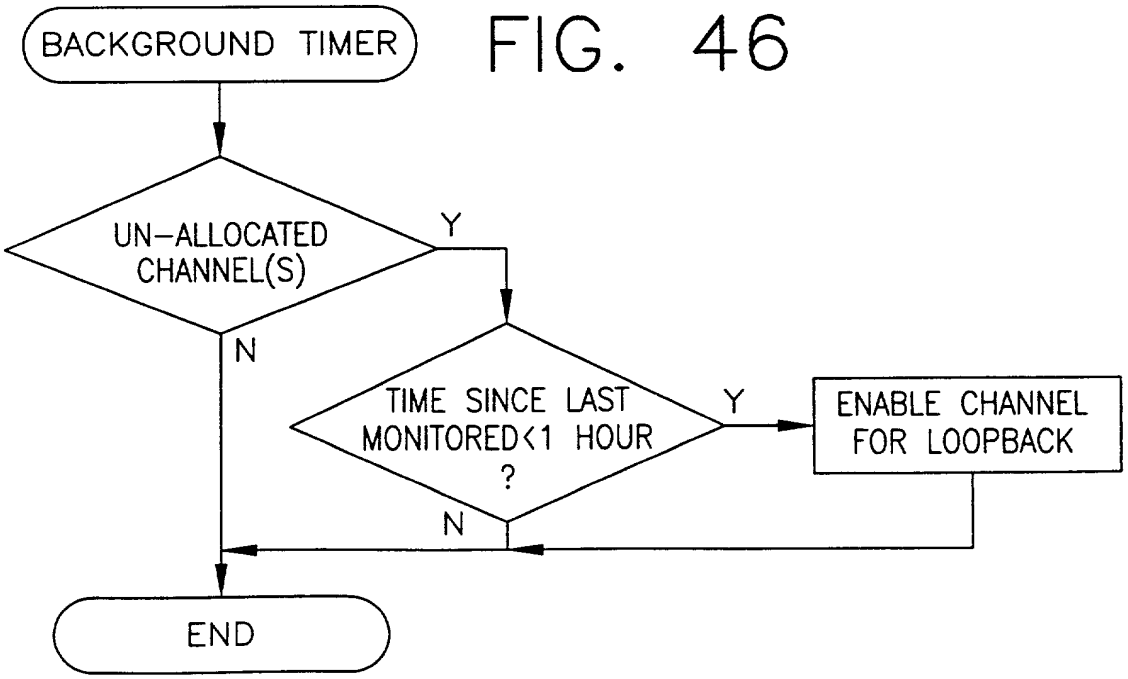

BACKGROUND TIMER
UN-ALLOCATED CHANNEL(S)
Y
N
TIME SINCE LAST MONITORED<1 HOUR ?
Y
N
ENABLE CHANNEL FOR LOOPBACK
END

FIG. 46

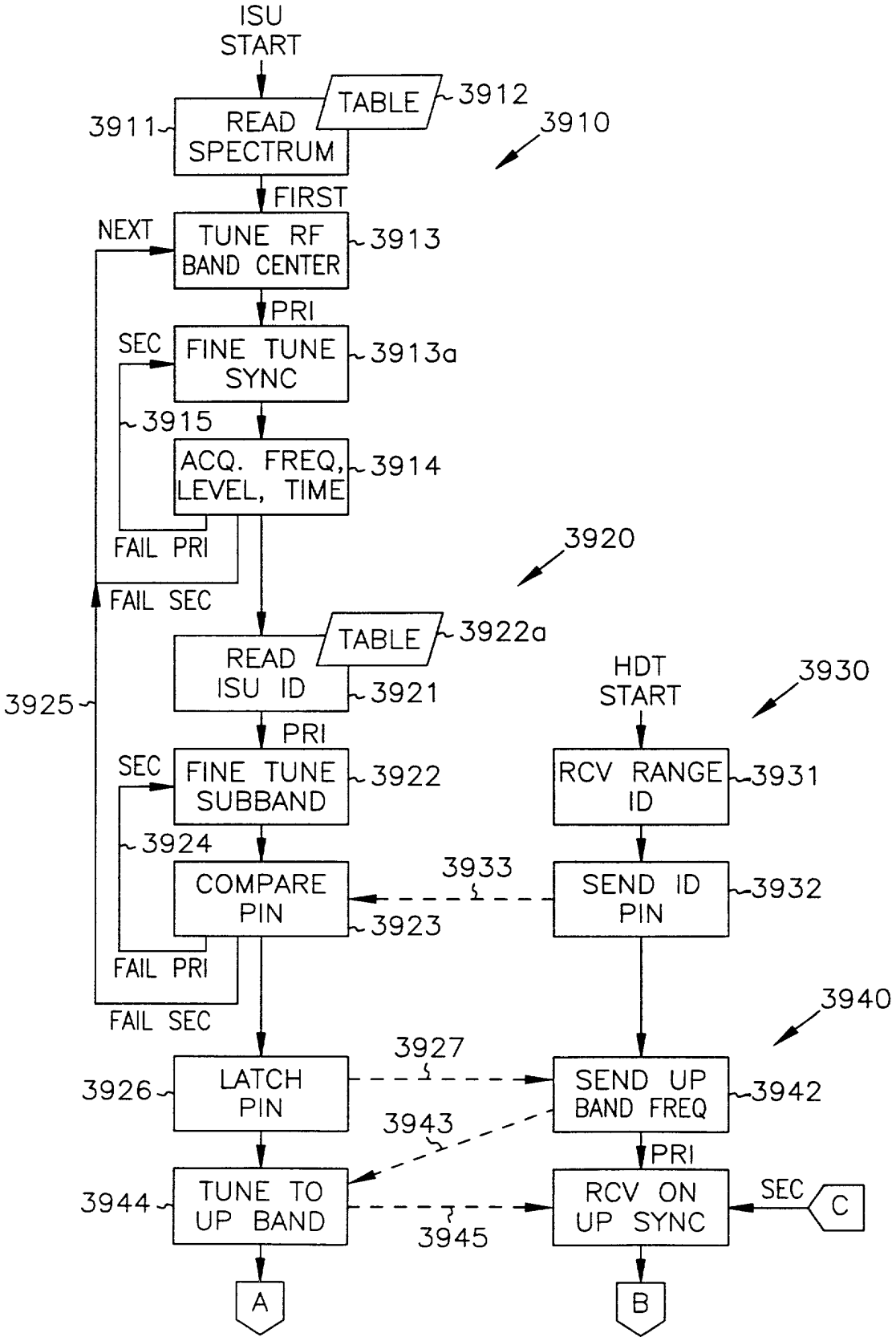

ISU START
TABLE
3912
3911
READ SPECTRUM
3910
FIRST
NEXT
TUNE RF BAND CENTER
3913
PRI
SEC
FINE TUNE SYNC
3913a
3915
ACQ. FREQ, LEVEL, TIME
3914
FAIL PRI
FAIL SEC
3920
TABLE
3922a
READ ISU ID
3921
3925
PRI
SEC
FINE TUNE SUBBAND
3922
3924
COMPARE PIN
3923
FAIL PRI
FAIL SEC
HDT START
3930
RCV RANGE ID
3931
3933
SEND ID PIN
3932
3940
3927
LATCH PIN
3926
SEND UP BAND FREQ
3942
3943
PRI
TUNE TO UP BAND
3944
RCV ON UP SYNC
SEC
C
3945
A
B

FIG. 47

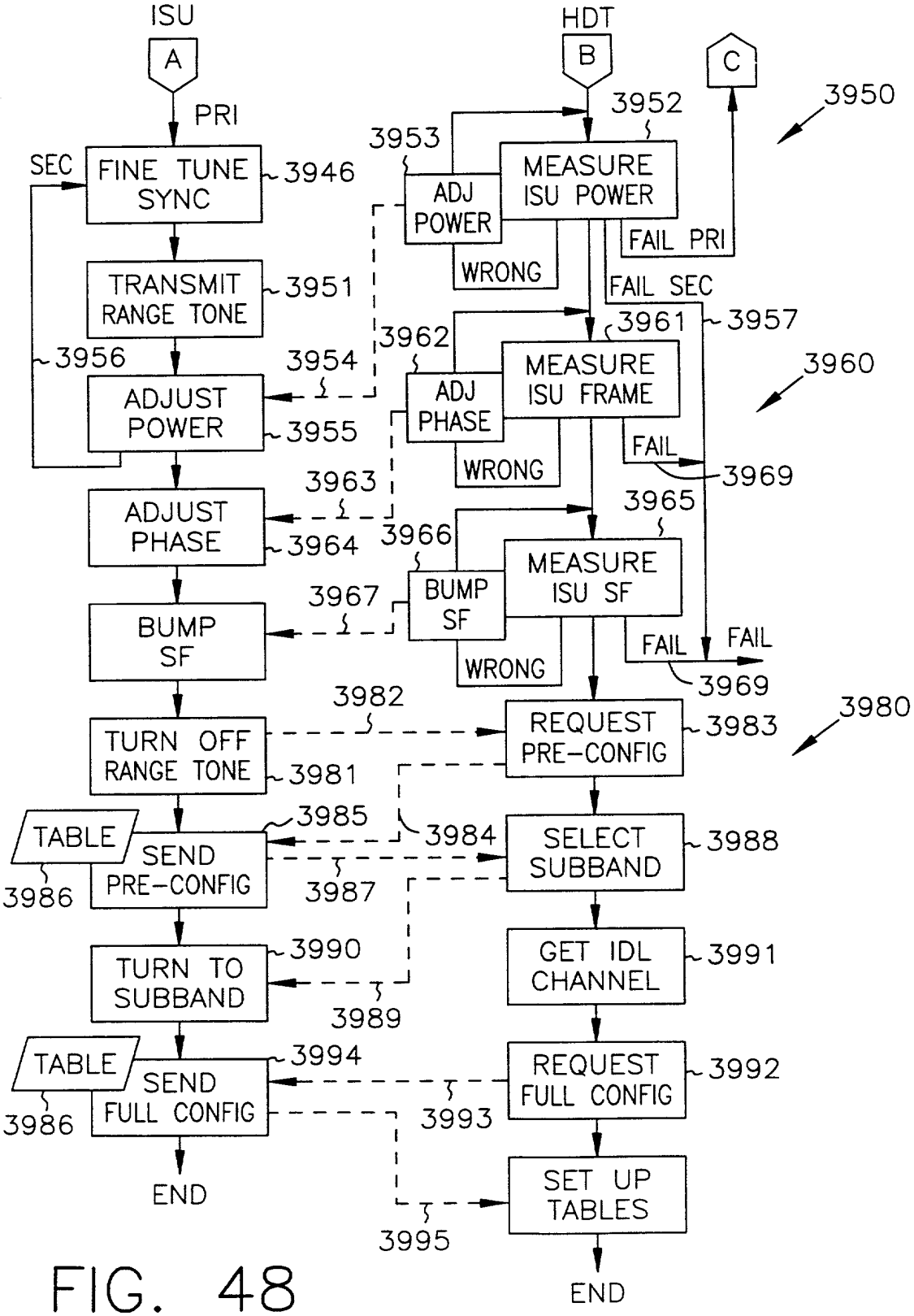

ISU
A
PRI
SEC
FINE TUNE SYNC
3946
TRANSMIT RANGE TONE
3951
3956
ADJUST POWER
3955
3954
ADJUST PHASE
3964
3963
BUMP SF
3967
TURN OFF RANGE TONE
3981
TABLE
SEND PRE-CONFIG
3986
3985
TURN TO SUBBAND
3990
3989
TABLE
SEND FULL CONFIG
3986
3994
END
HDT
B
C
3950
3952
3953
MEASURE ISU POWER
ADJ POWER
WRONG
FAIL PRI
FAIL SEC
3961
3957
3962
MEASURE ISU FRAME
ADJ PHASE
WRONG
FAIL
3969
3960
3965
3966
MEASURE ISU SF
BUMP SF
WRONG
FAIL
FAIL
3969
3982
REQUEST PRE-CONFIG
3983
3980
3984
SELECT SUBBAND
3988
3987
GET IDL CHANNEL
3991
REQUEST FULL CONFIG
3992
3993
SET UP TABLES
3995
END

FIG. 48

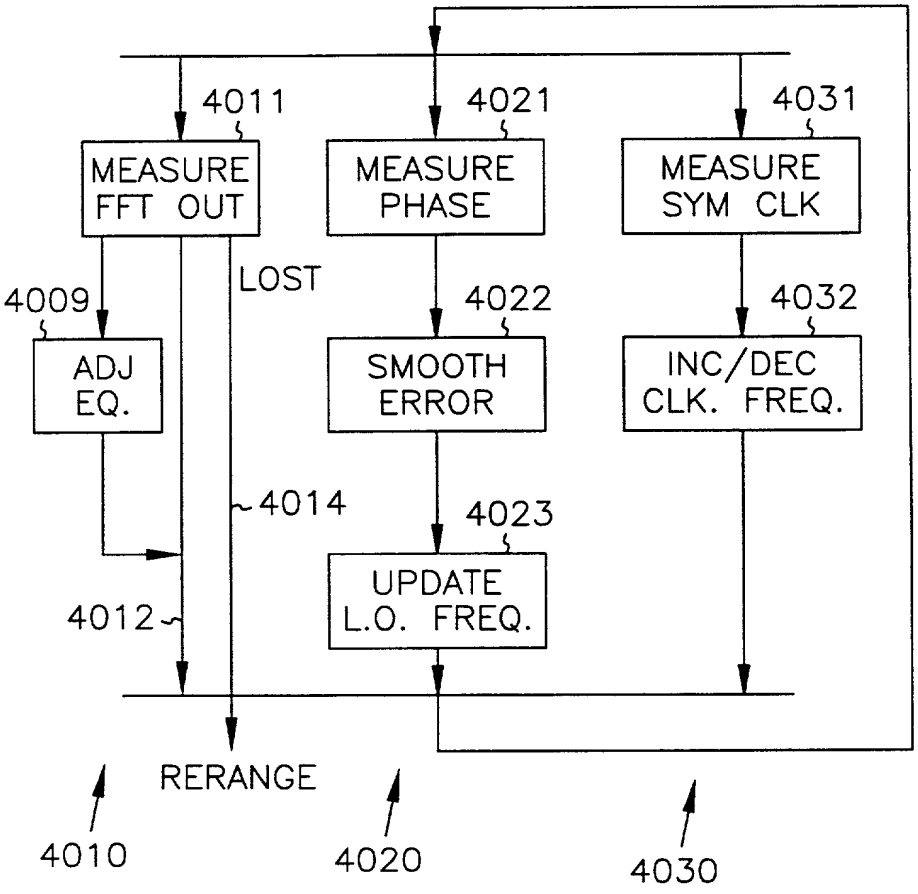

4011
4021
4031
MEASURE FFT OUT
MEASURE PHASE
MEASURE SYM CLK
LOST
4009
4022
4032
ADJ EQ.
SMOOTH ERROR
INC/DEC CLK. FREQ.
4014
4023
UPDATE L.O. FREQ.
4012
RERANGE
4010
4020
4030

FIG. 49

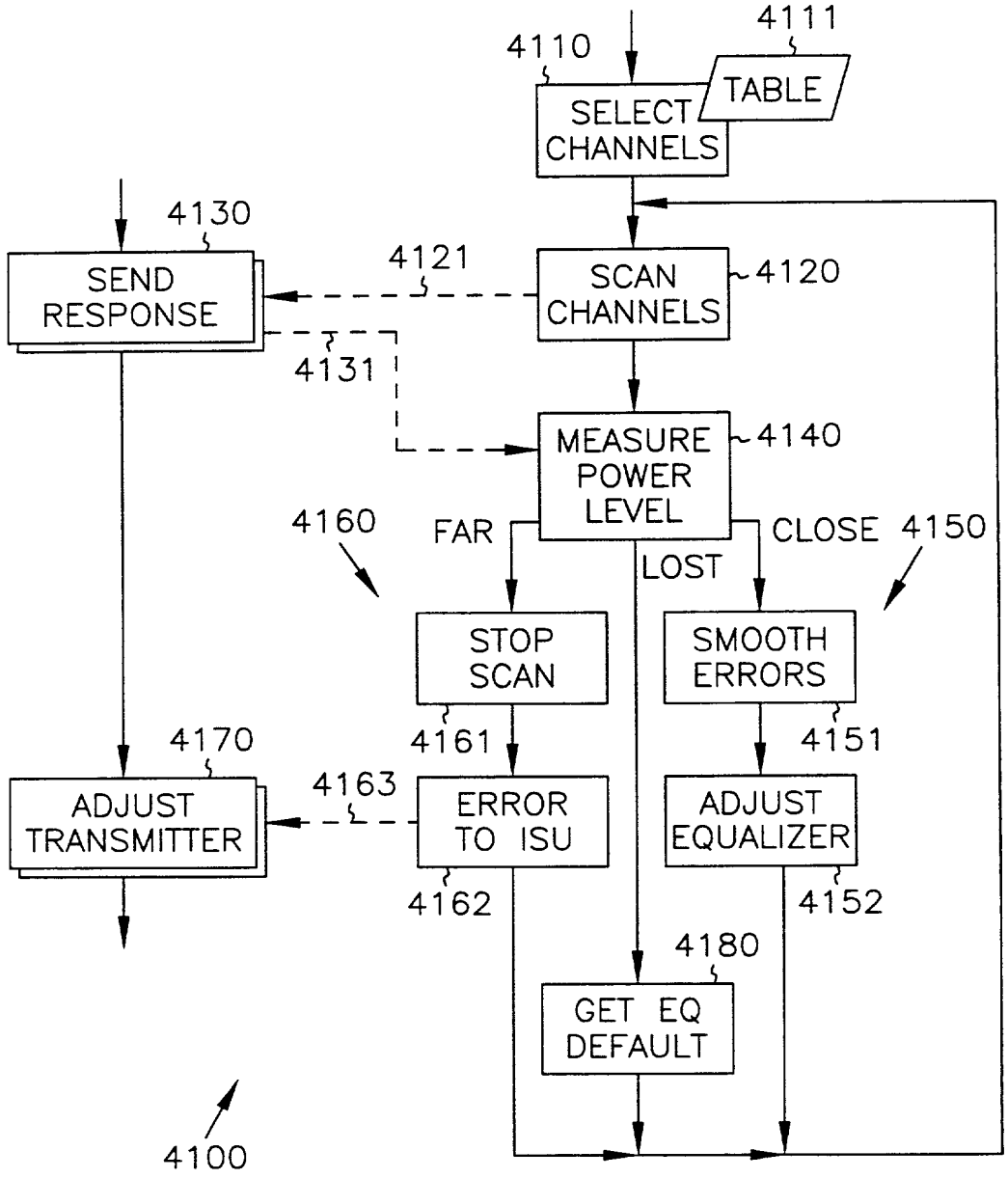

4111
4110
TABLE
SELECT CHANNELS
4130
SEND RESPONSE
4121
SCAN CHANNELS
4120
4131
MEASURE POWER LEVEL
4140
4160
FAR
CLOSE
4150
LOST
STOP SCAN
SMOOTH ERRORS
4161
4151
4170
4163
ADJUST TRANSMITTER
ERROR TO ISU
ADJUST EQUALIZER
4162
4152
4180
GET EQ DEFAULT
4100

FIG. 50

20170150154

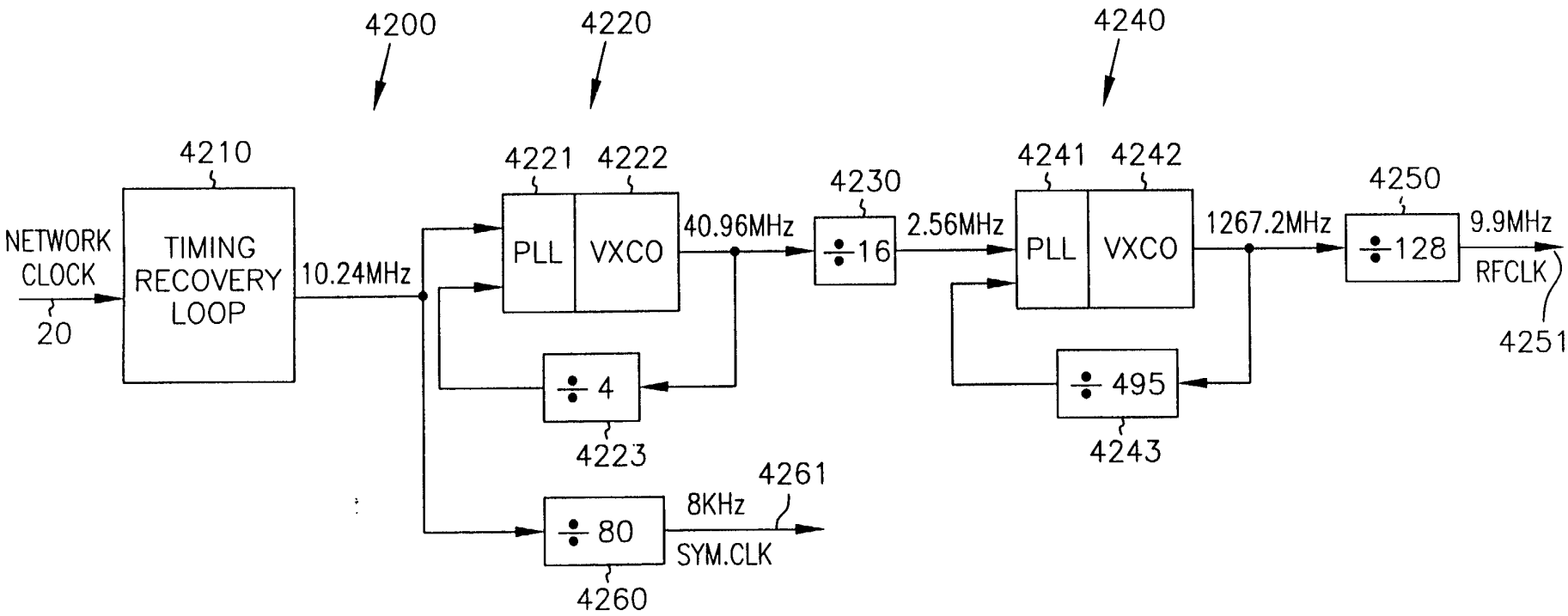


FIG. 51

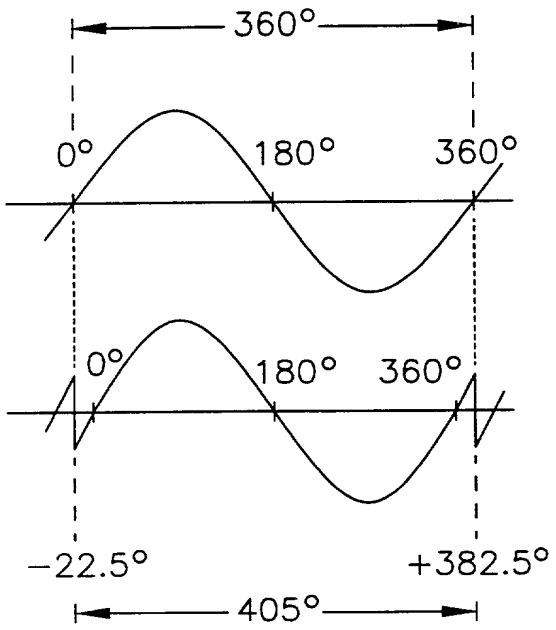

360°
0°
180°
360°
0°
180°
360°
−22.5°
+382.5°
405°

FIG. 52

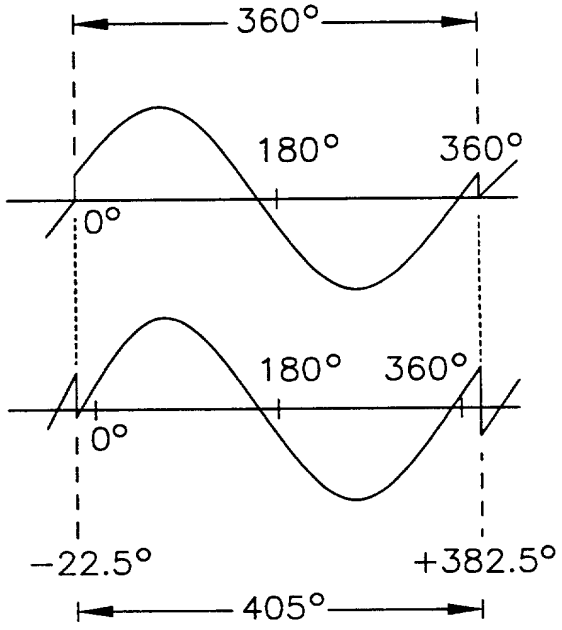

360°
180°
360°
0°
180°
360°
0°
−22.5°
+382.5°
405°

FIG. 53

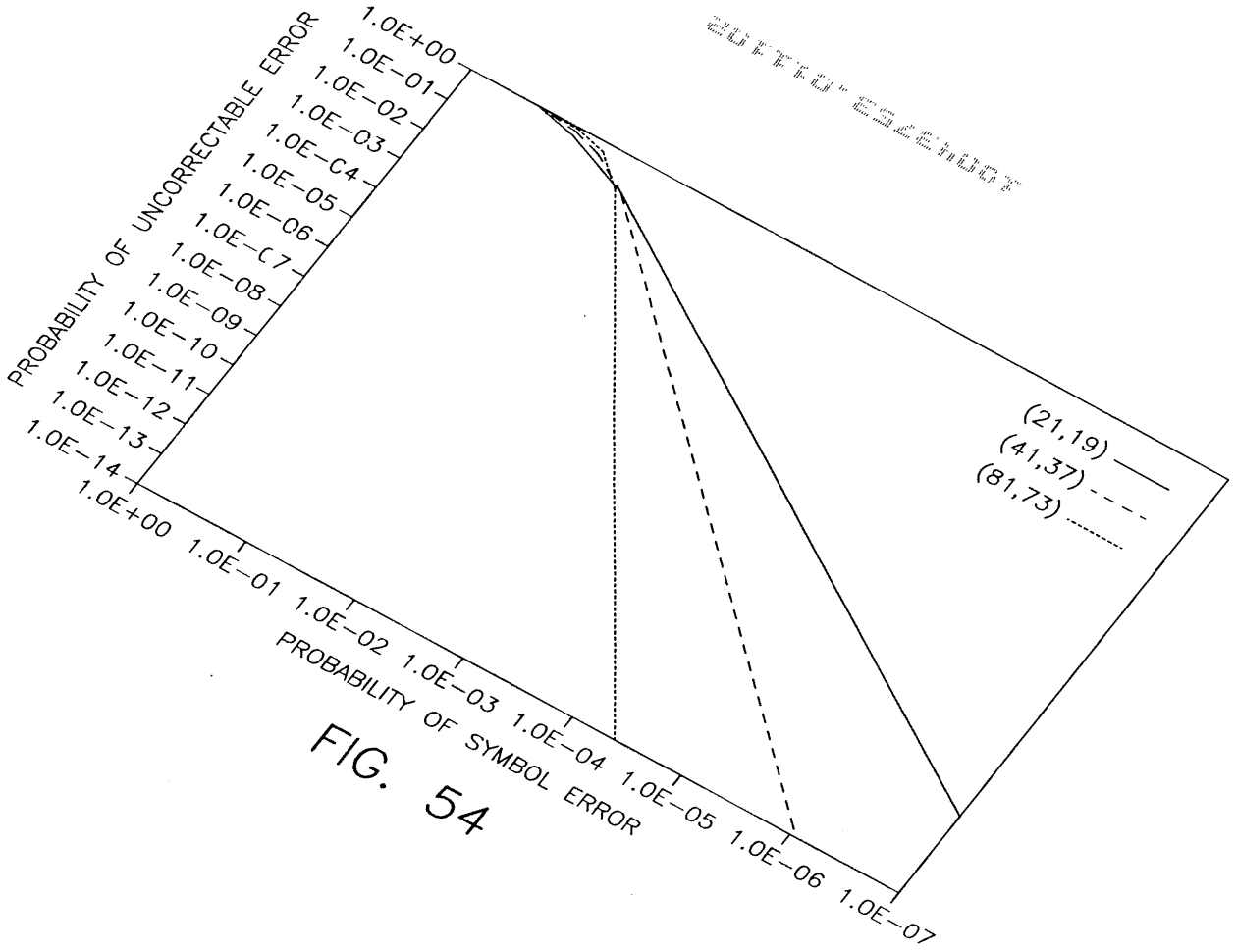

PROBABILITY OF UNCORRECTABLE ERROR
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
1.0E-09
1.0E-10
1.0E-11
1.0E-12
1.0E-13
1.0E-14
1.0E+00 1.0E-01 1.0E-02 1.0E-03 1.0E-04 1.0E-05 1.0E-06 1.0E-07
PROBABILITY OF SYMBOL ERROR
(21,19)
(41,37)
(81,73)

FIG. 54

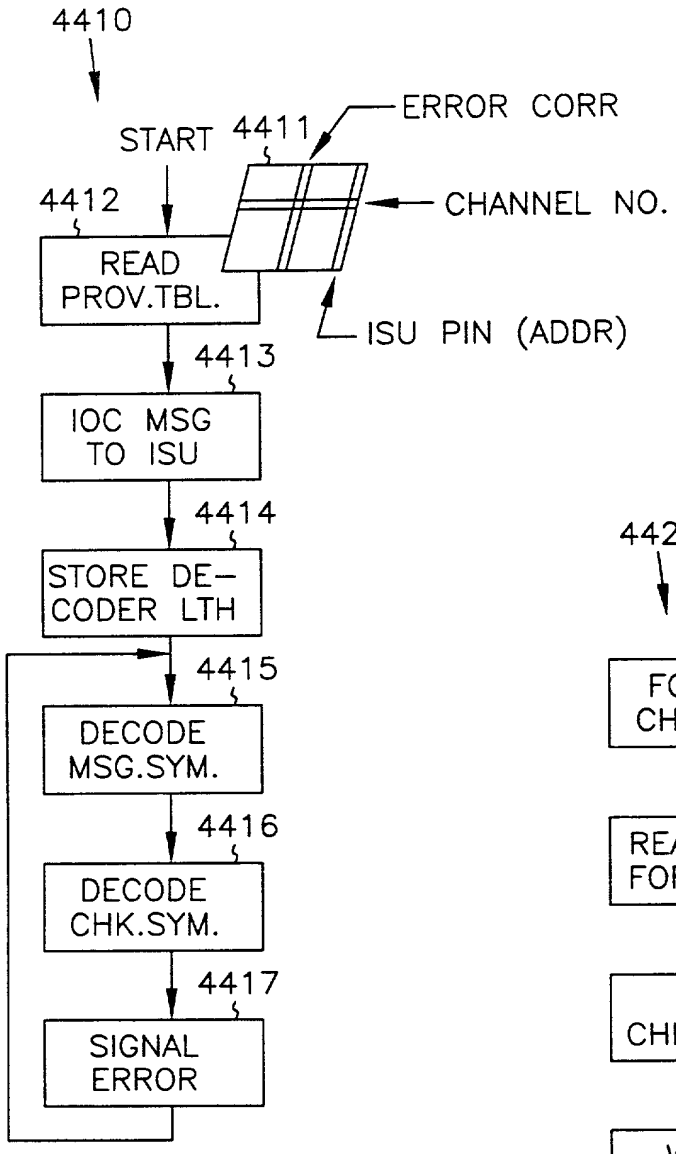

4410
START
4411
ERROR CORR
4412
CHANNEL NO.
READ PROV.TBL.
ISU PIN (ADDR)
4413
IOC MSG TO ISU
4414
STORE DE-CODER LTH
4415
DECODE MSG.SYM.
4416
DECODE CHK.SYM.
4417
SIGNAL ERROR

FIG. 55

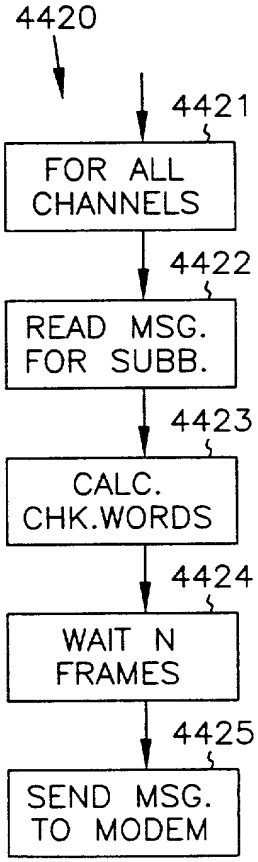

4420
4421
FOR ALL CHANNELS
4422
READ MSG. FOR SUBB.
4423
CALC. CHK.WORDS
4424
WAIT N FRAMES
4425
SEND MSG. TO MODEM

FIG. 56

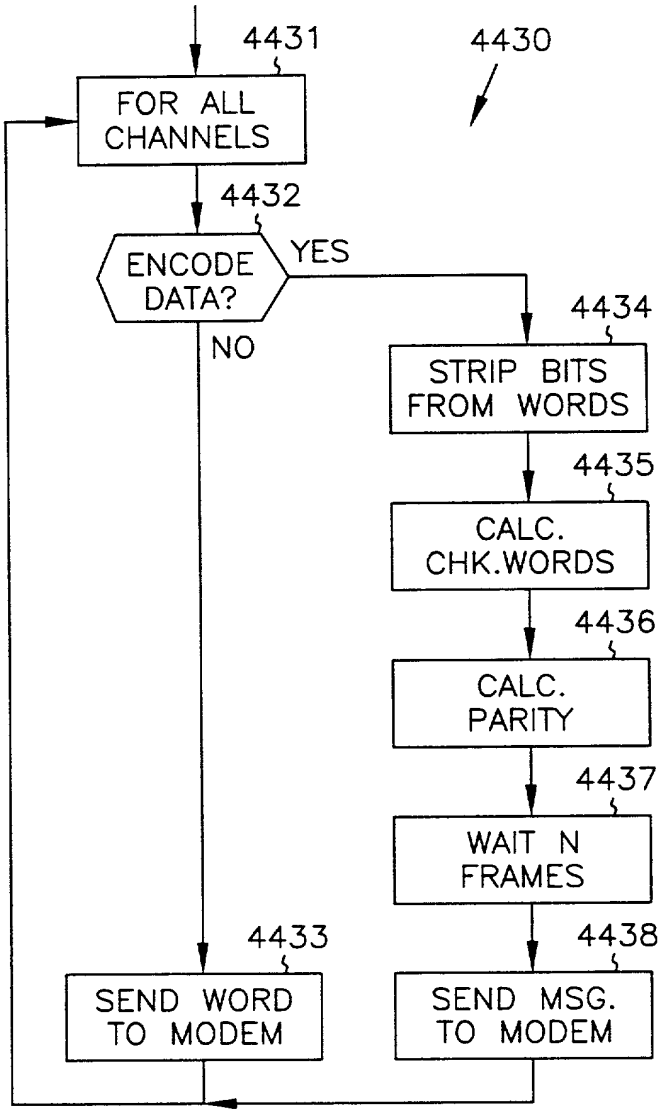

4431
4430
FOR ALL CHANNELS
4432
ENCODE DATA?
YES
NO
4434
STRIP BITS FROM WORDS
4435
CALC. CHK.WORDS
4436
CALC. PARITY
4437
WAIT N FRAMES
4433
SEND WORD TO MODEM
4438
SEND MSG. TO MODEM

FIG. 57

20170215204907

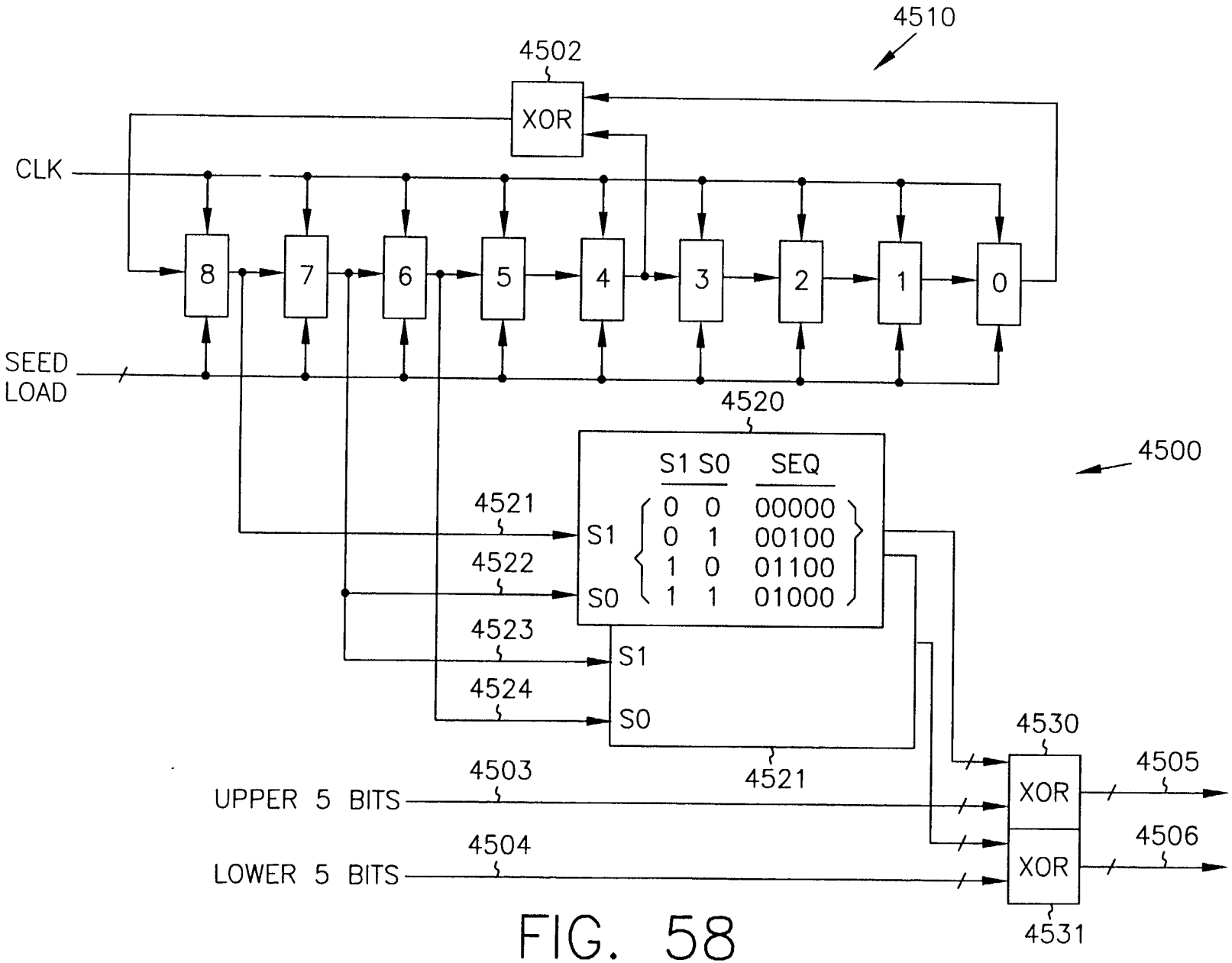


FIG. 58

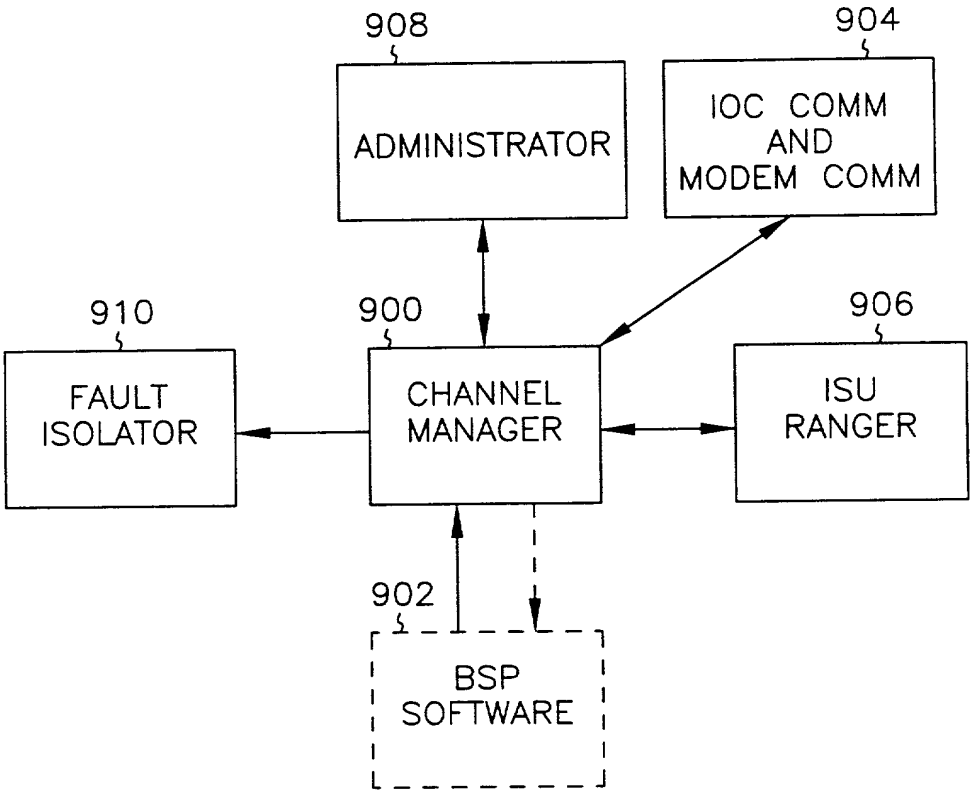

908
ADMINISTRATOR
904
IOC COMM
AND
MODEM COMM
910
FAULT
ISOLATOR
900
CHANNEL
MANAGER
906
ISU
RANGER
902
BSP
SOFTWARE

FIG. 59

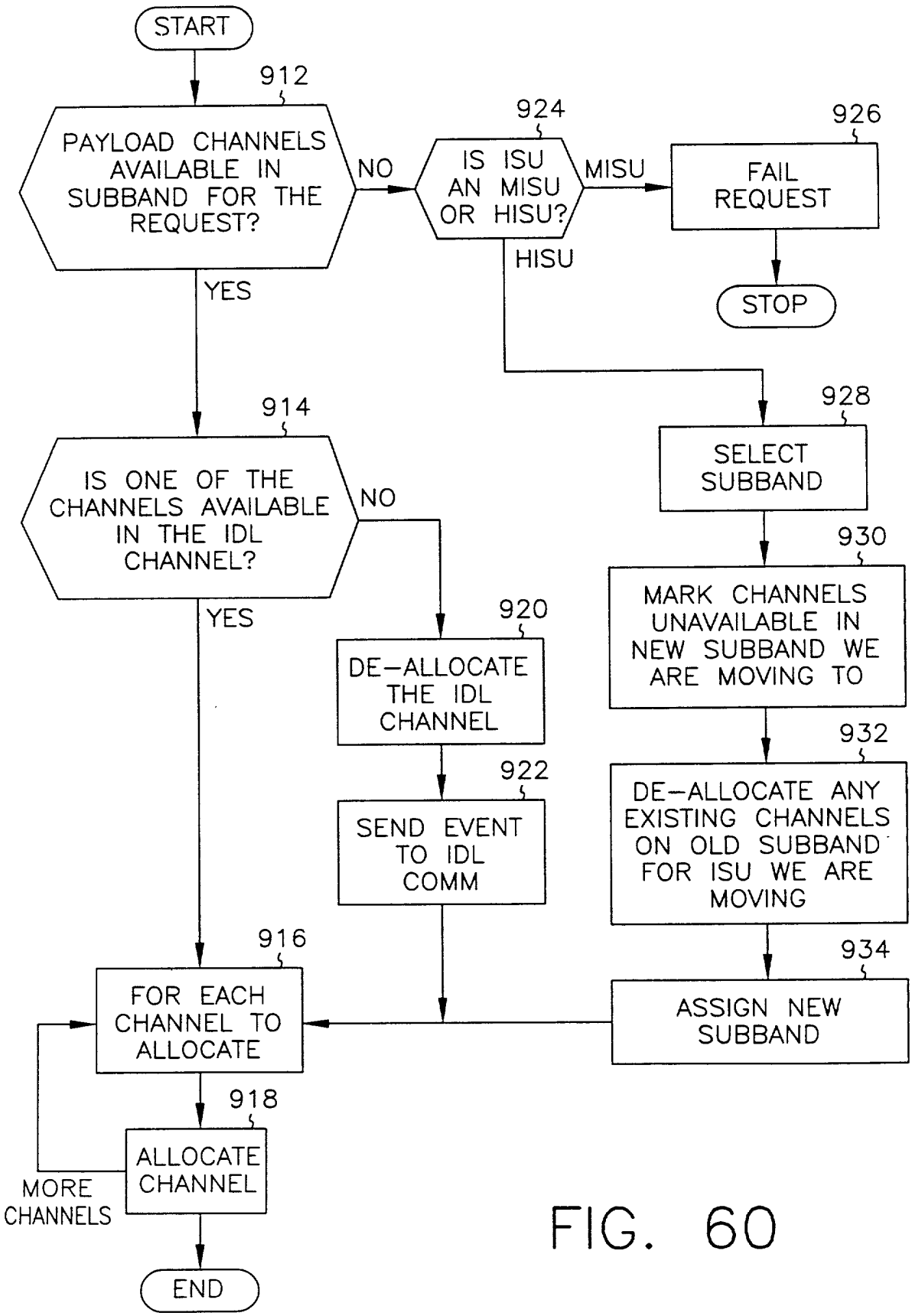

START
912
PAYLOAD CHANNELS AVAILABLE IN SUBBAND FOR THE REQUEST?
NO
924
IS ISU AN MISU OR HISU?
MISU
926
FAIL REQUEST
STOP
HISU
YES
914
IS ONE OF THE CHANNELS AVAILABLE IN THE IDL CHANNEL?
NO
YES
920
DE-ALLOCATE THE IDL CHANNEL
922
SEND EVENT TO IDL COMM
928
SELECT SUBBAND
930
MARK CHANNELS UNAVAILABLE IN NEW SUBBAND WE ARE MOVING TO
932
DE-ALLOCATE ANY EXISTING CHANNELS ON OLD SUBBAND FOR ISU WE ARE MOVING
934
ASSIGN NEW SUBBAND
916
FOR EACH CHANNEL TO ALLOCATE
918
ALLOCATE CHANNEL
MORE CHANNELS
END

FIG. 60

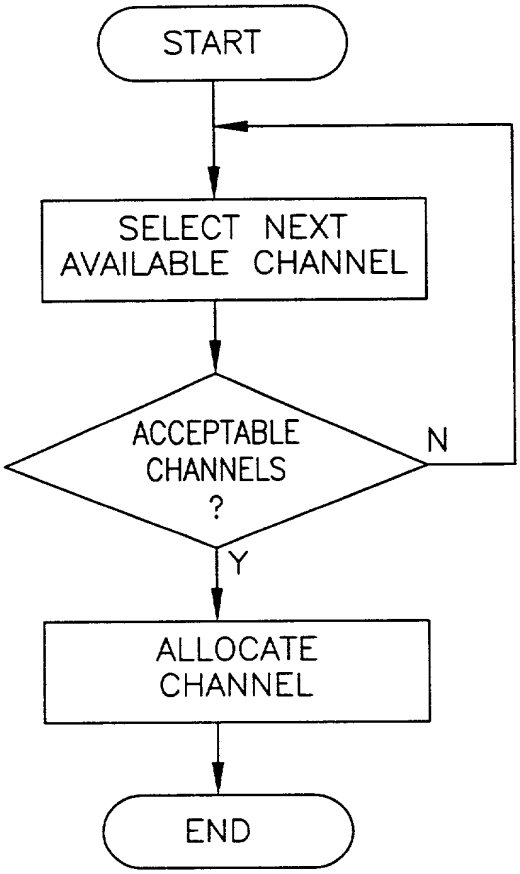

START
SELECT NEXT AVAILABLE CHANNEL
ACCEPTABLE CHANNELS ?
N
Y
ALLOCATE CHANNEL
END

FIG. 61

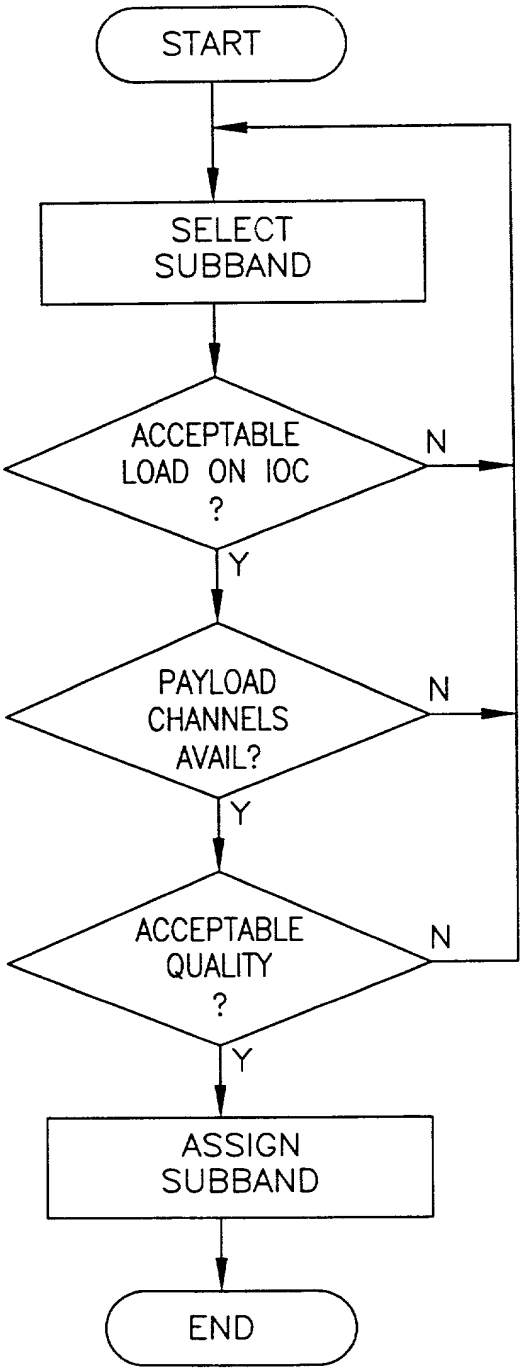

START
SELECT SUBBAND
ACCEPTABLE LOAD ON IOC ?
N
Y
PAYLOAD CHANNELS AVAIL?
N
Y
ACCEPTABLE QUALITY ?
N
Y
ASSIGN SUBBAND
END

FIG. 62

EXHIBIT 1 - PAGE 1 OF 1

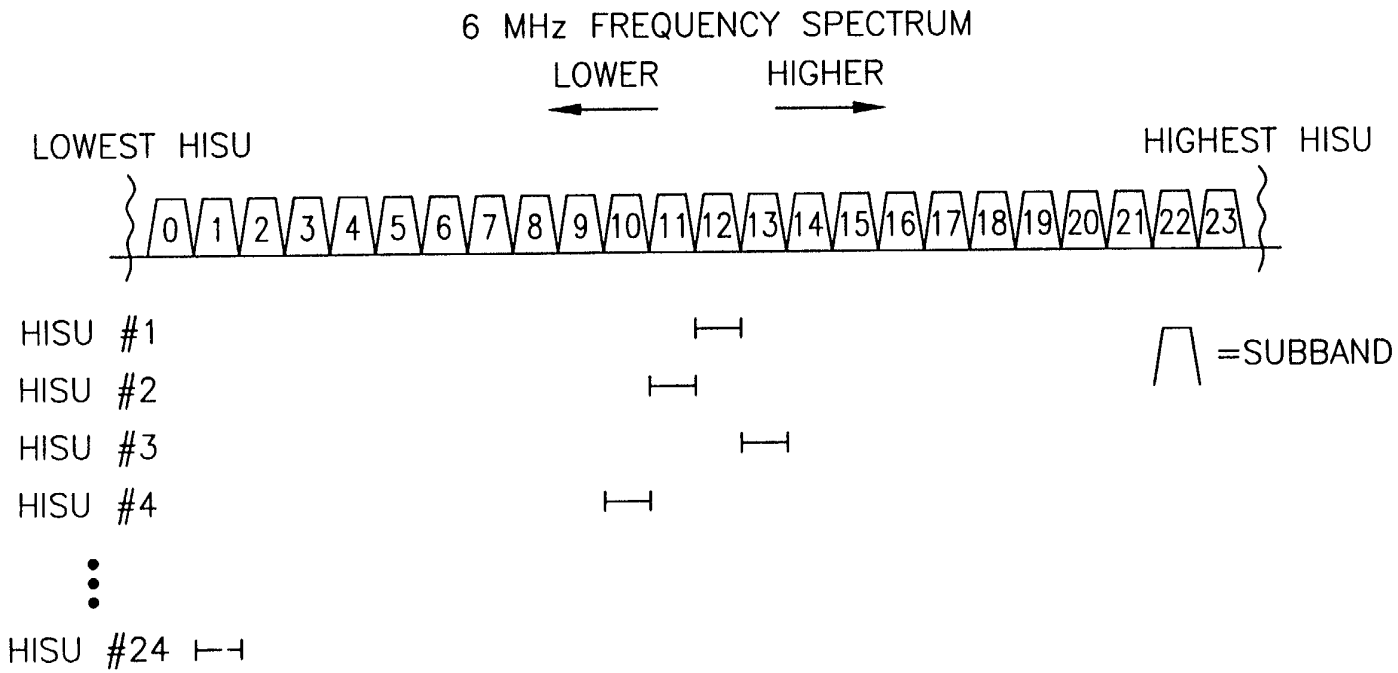


FIG. 63

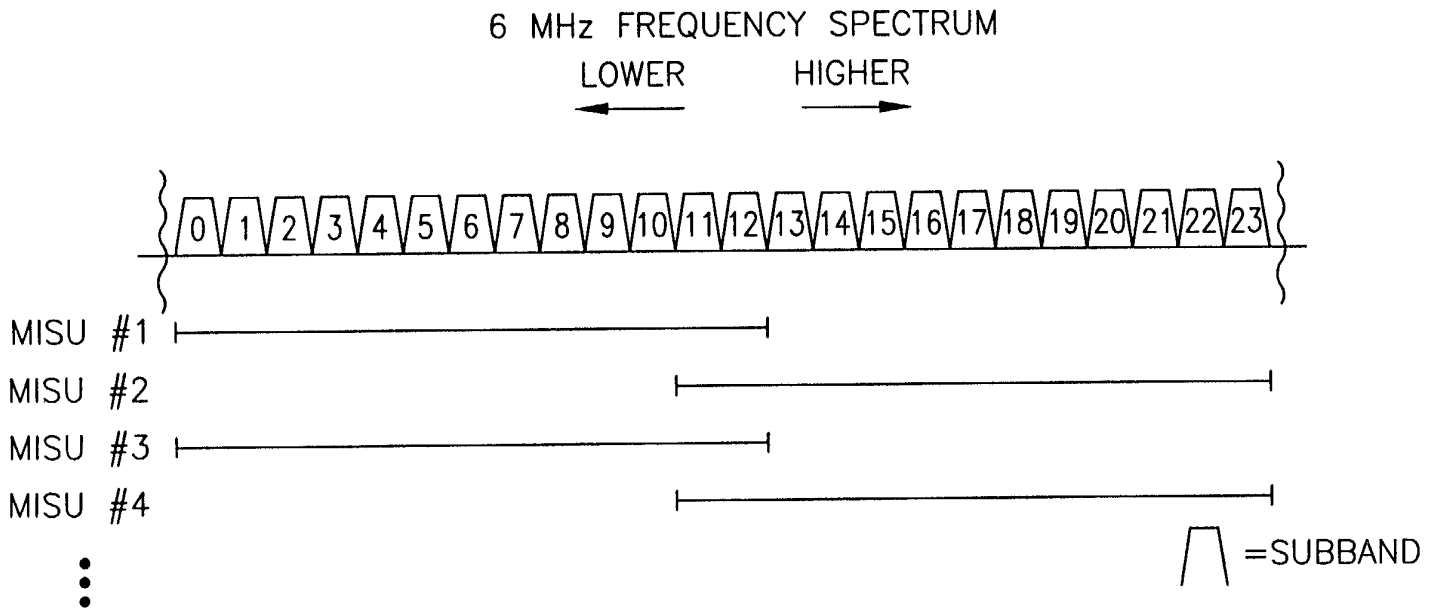

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
MISU #1
MISU #2
MISU #3
MISU #4
=SUBBAND

FIG. 64

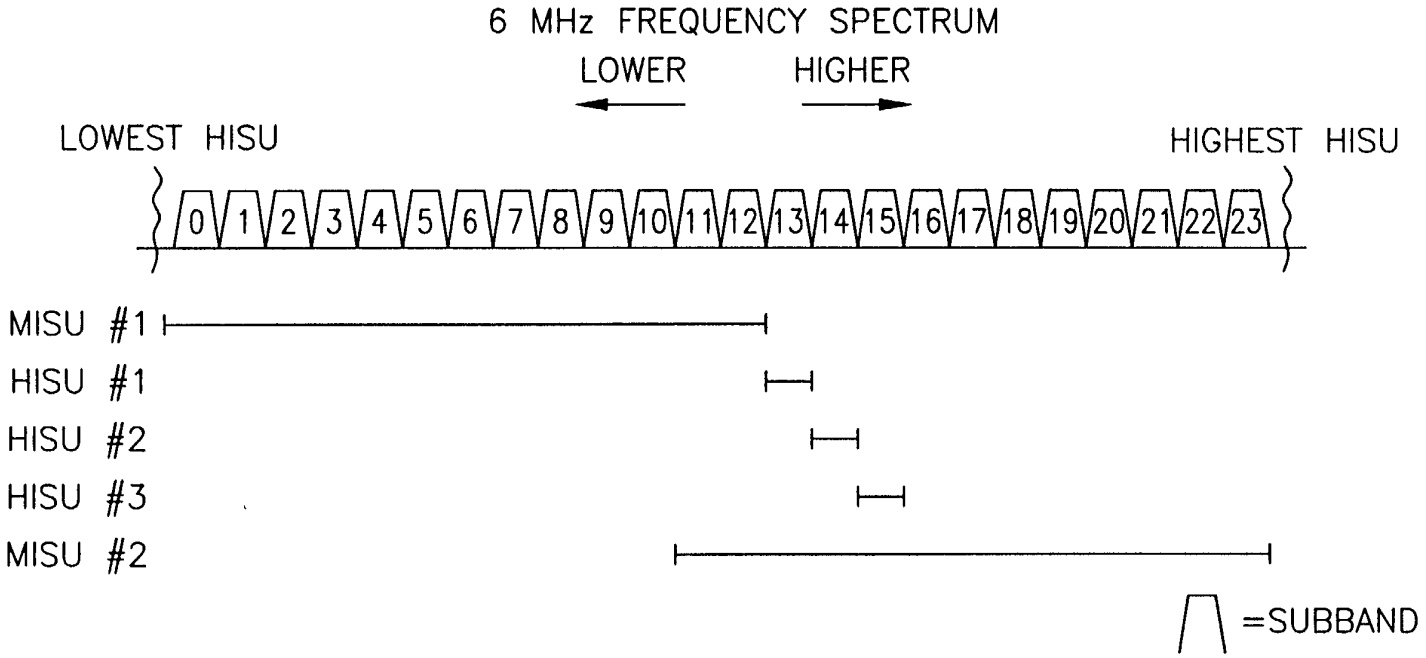

6 MHz FREQUENCY SPECTRUM
LOWER
HIGHER
LOWEST HISU
HIGHEST HISU
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
MISU #1
HISU #1
HISU #2
HISU #3
MISU #2
=SUBBAND

FIG. 65

SCREENSHOT

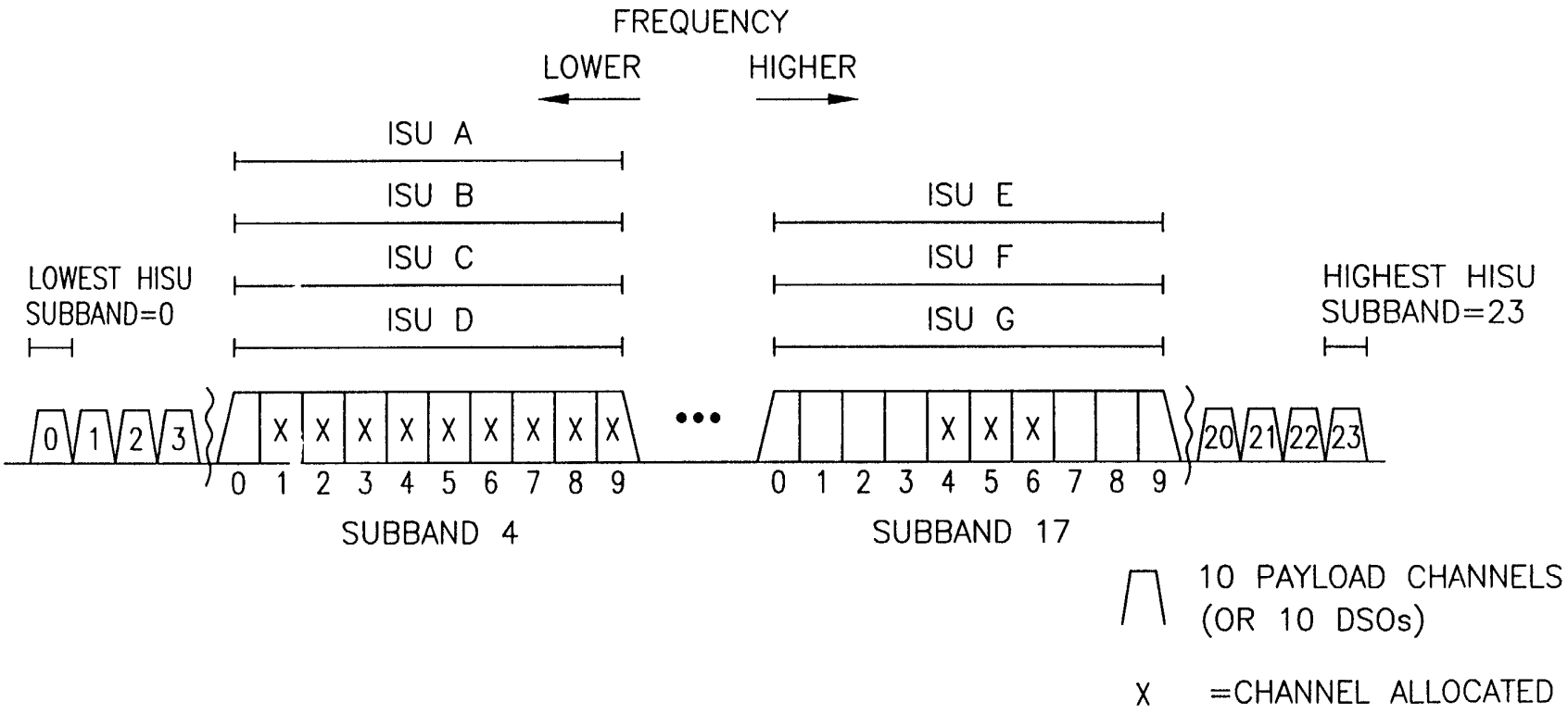


FIG. 66

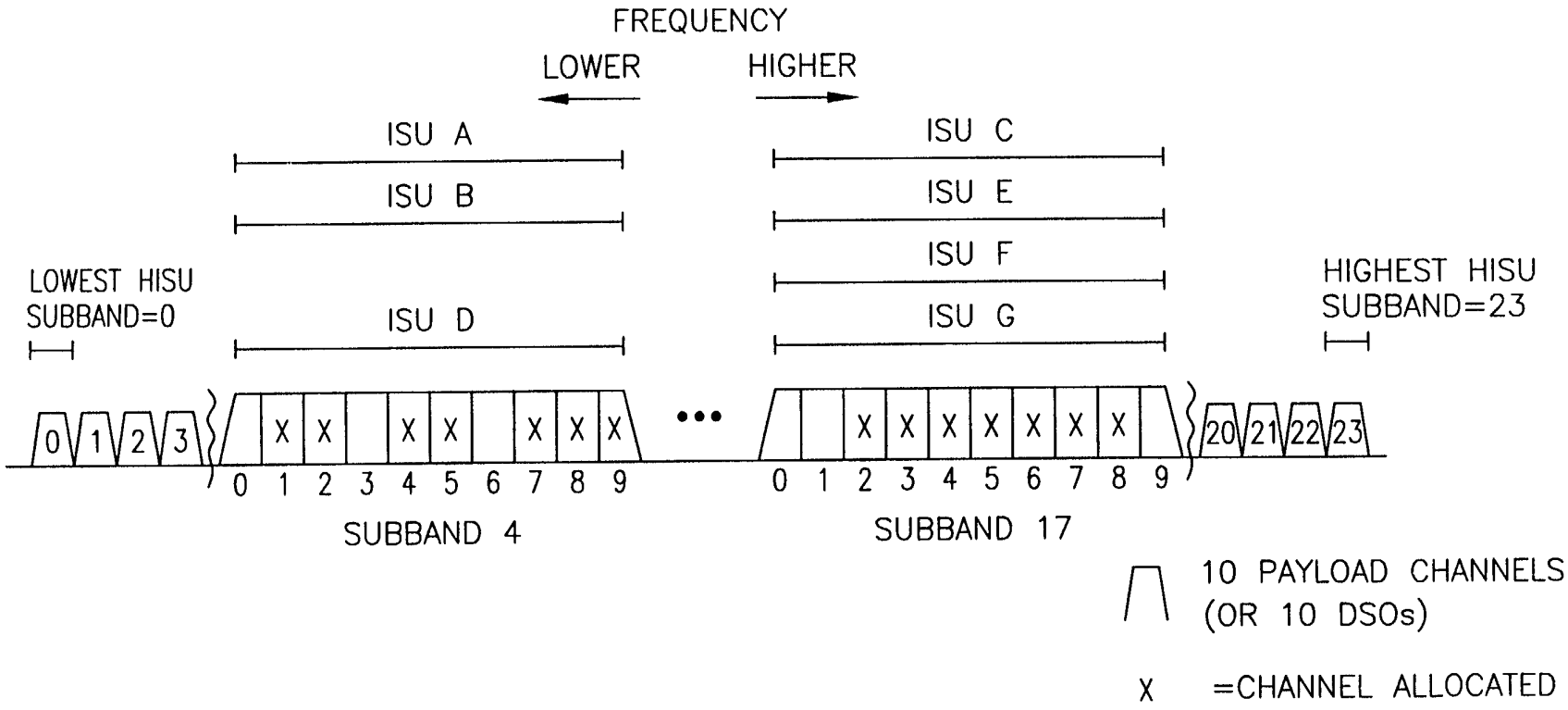

FREQUENCY
LOWER
HIGHER
ISU A
ISU B
ISU C
ISU E
ISU F
ISU D
ISU G
LOWEST HISU
SUBBAND=0
HIGHEST HISU
SUBBAND=23
0 1 2 3
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 4
X X X X X X X
0 1 2 3 4 5 6 7 8 9
SUBBAND 17
20 21 22 23
10 PAYLOAD CHANNELS
(OR 10 DSOs)
X =CHANNEL ALLOCATED

FIG. 67

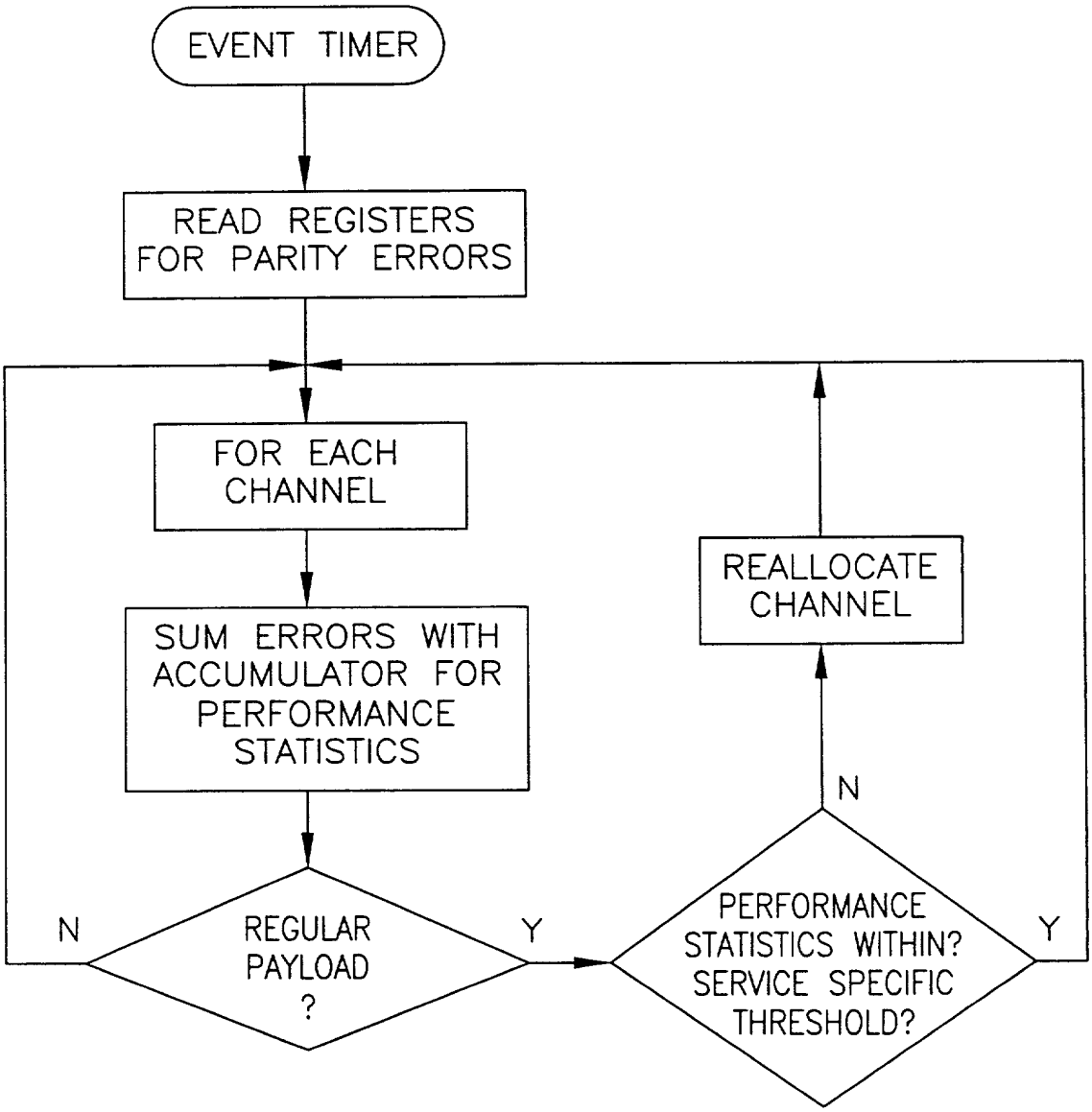

EVENT TIMER
READ REGISTERS FOR PARITY ERRORS
FOR EACH CHANNEL
SUM ERRORS WITH ACCUMULATOR FOR PERFORMANCE STATISTICS
REGULAR PAYLOAD ?
N
Y
PERFORMANCE STATISTICS WITHIN? SERVICE SPECIFIC THRESHOLD?
N
Y
REALLOCATE CHANNEL

FIG. 68

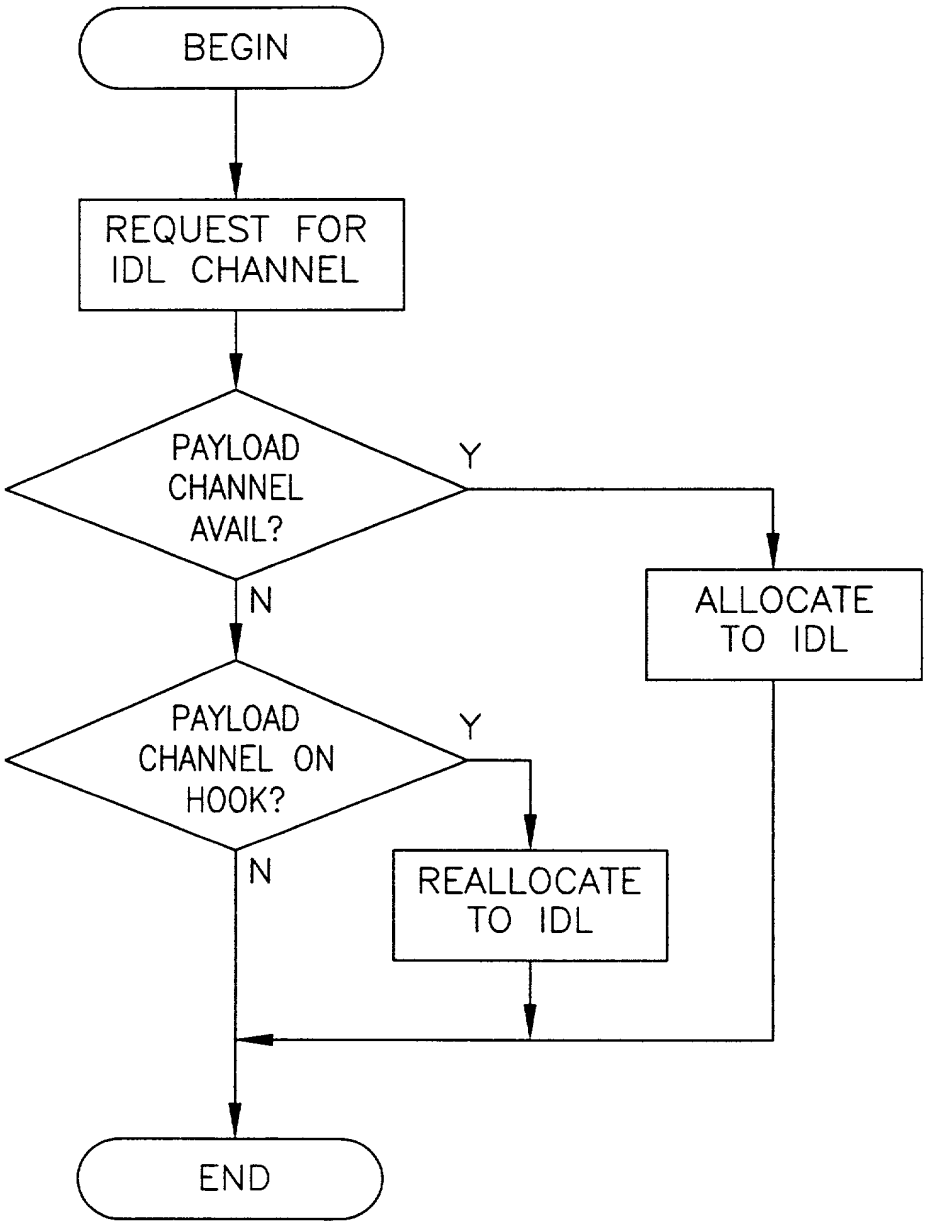

BEGIN
REQUEST FOR IDL CHANNEL
PAYLOAD CHANNEL AVAIL?
Y
N
ALLOCATE TO IDL
PAYLOAD CHANNEL ON HOOK?
Y
N
REALLOCATE TO IDL
END

FIG. 69

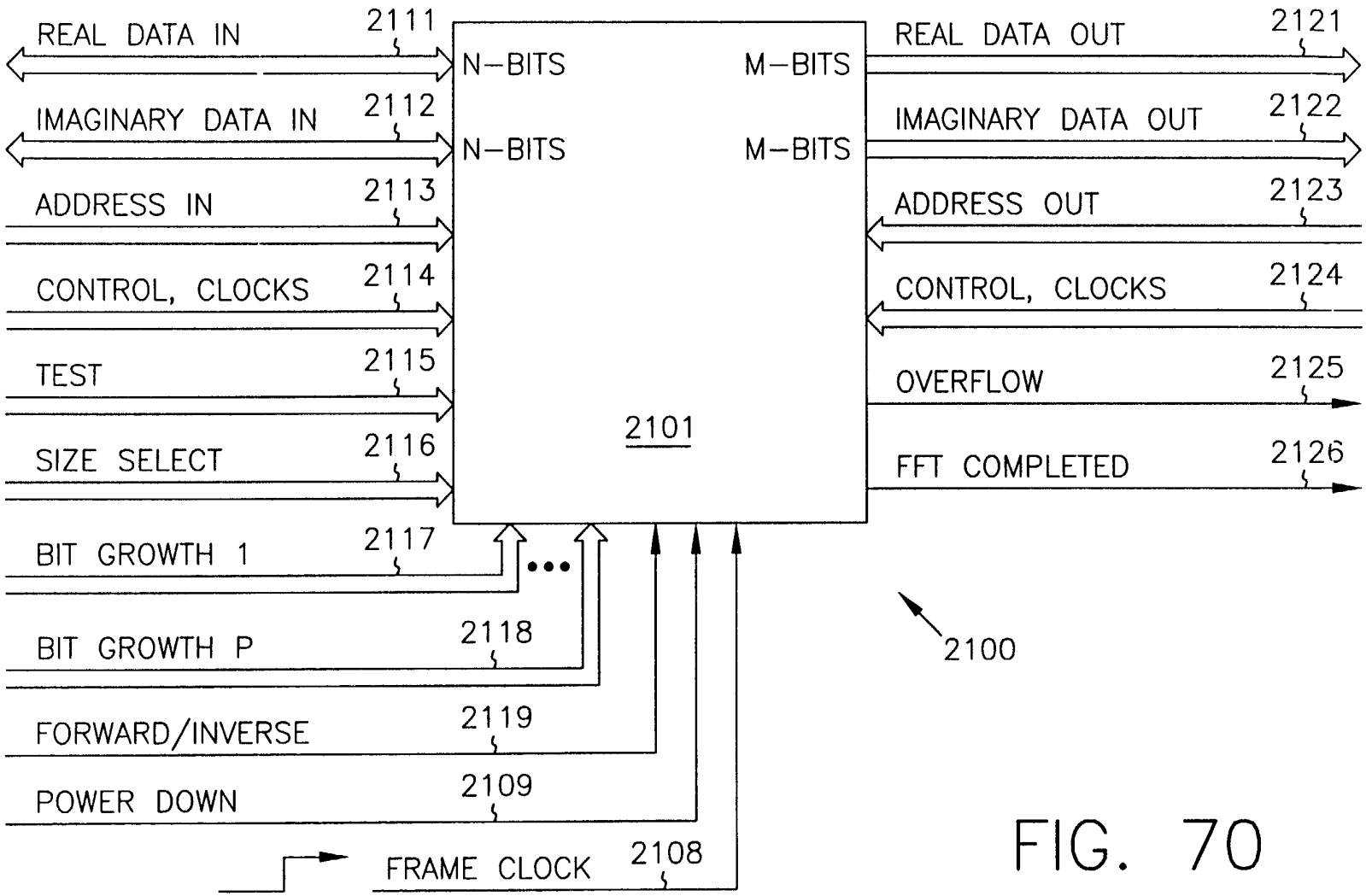

REAL DATA IN
2111
N-BITS
M-BITS
REAL DATA OUT
2121
IMAGINARY DATA IN
2112
N-BITS
M-BITS
IMAGINARY DATA OUT
2122
ADDRESS IN
2113
ADDRESS OUT
2123
CONTROL, CLOCKS
2114
CONTROL, CLOCKS
2124
TEST
2115
OVERFLOW
2125
2101
SIZE SELECT
2116
FFT COMPLETED
2126
BIT GROWTH 1
2117
BIT GROWTH P
2118
2100
FORWARD/INVERSE
2119
POWER DOWN
2109
FRAME CLOCK
2108

FIG. 70

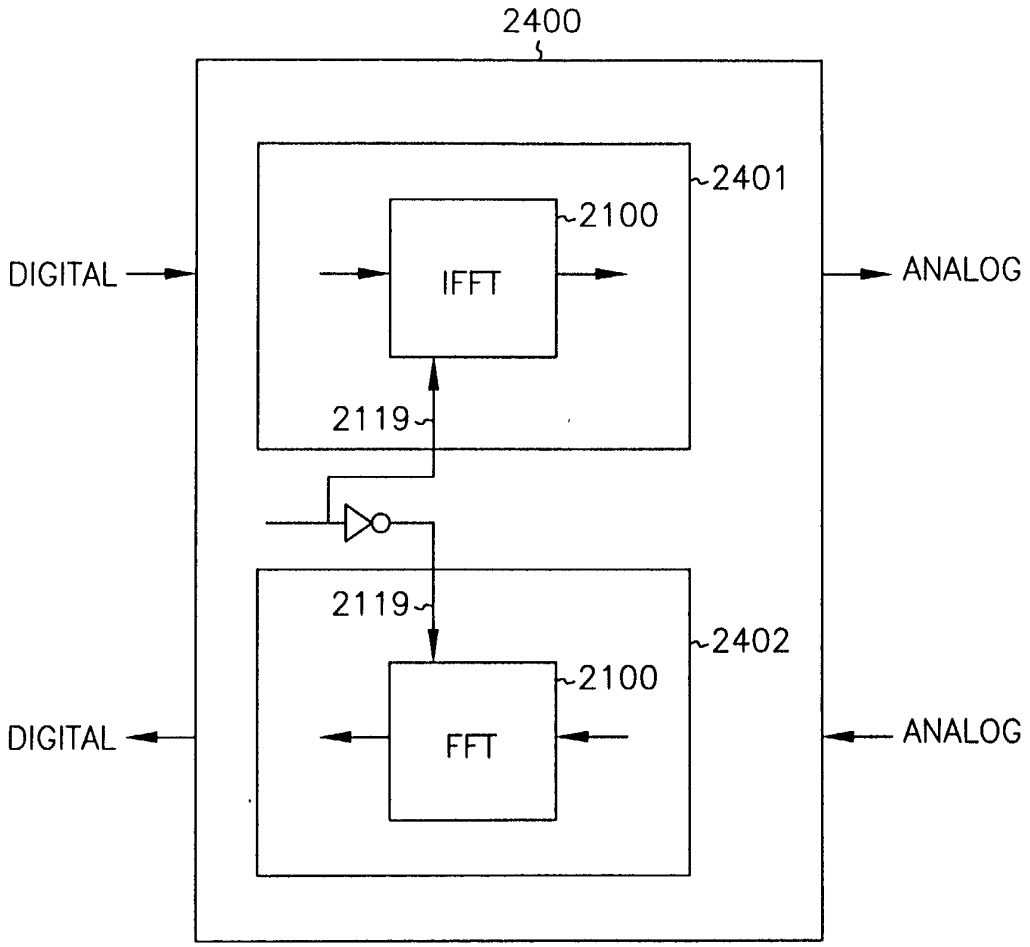

2400
2401
2100
IFFT
DIGITAL
ANALOG
2119
2119
2402
2100
FFT
DIGITAL
ANALOG

FIG. 71

Patent Search

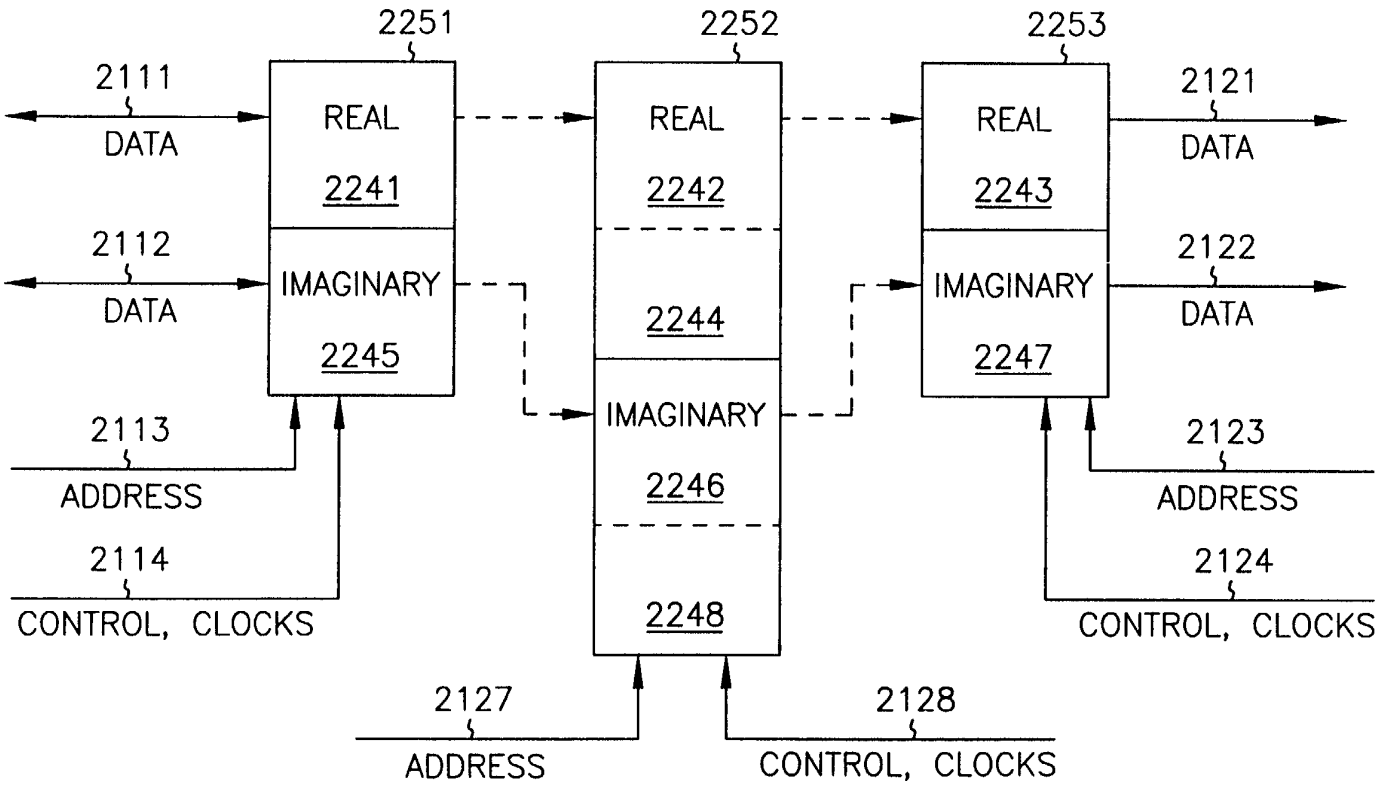


FIG. 72

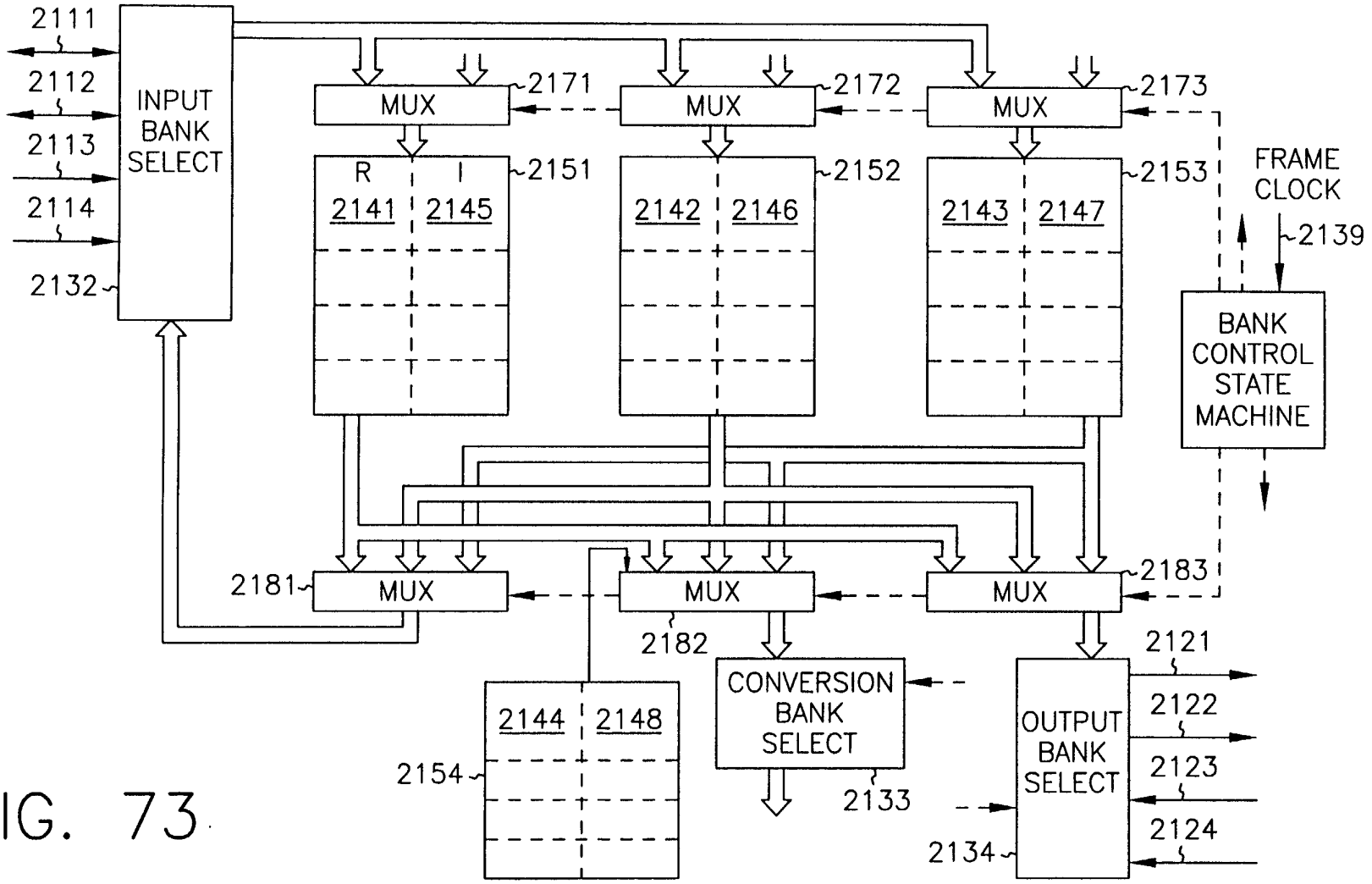
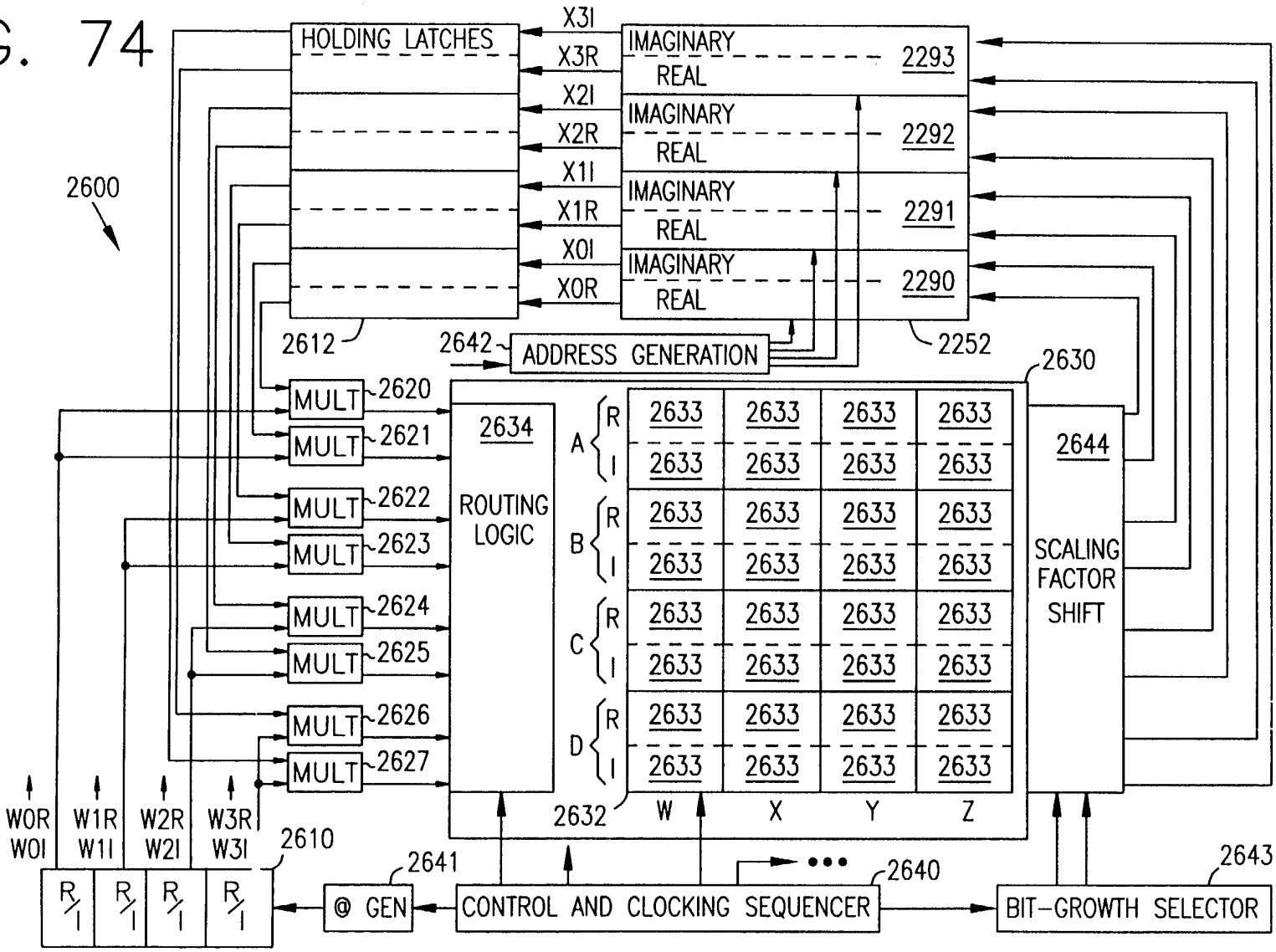

2111
2112
2113
2114
2132
INPUT BANK SELECT
MUX
2171
MUX
2172
MUX
2173
R
I
2141
2145
2151
2142
2146
2152
2143
2147
2153
FRAME CLOCK
2139
BANK CONTROL STATE MACHINE
2181
MUX
MUX
MUX
2183
2182
2121
2144
2148
2154
CONVERSION BANK SELECT
2133
OUTPUT BANK SELECT
2122
2123
2124
2134

FIG. 73

Sheet 70 of 85

FIG. 74



THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

CO

AWR=WR AWI =WI	AXR =XR AXI =XI	AYR =YR AYI =YI	AZR =ZR AZI =ZI
BWR=WR BWI =WI	BXR=XR BXI =XI	BYR =YR BYI =YI	BZR=ZR BZI =ZI
CWR=WR CWI =WI	CXR=XR CXI =XI	CYR =YR CYI =YI	CZR=ZR CZI =ZI
DWR=WR DWI =WI	DXR=XR DXI =XI	DYR =YR DYI =YI	DZR=ZR DZI =ZI

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FIG. 75

CI

AWR=AWR −WI AWI=AWI +WR	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR −ZI DZI=DZI +ZR

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2800

FIG. 76

C2

AWR=AWR +WR AWI=AWI +WI	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR −ZI AZI=AZI +ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR −ZI BZI=BZI +ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR −ZI CZI=CZI +ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR −ZI DZI=DZI +ZR

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FIG. 77

C3

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XR AXI=AXI +XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XR BXI=BXI +XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XR CXI=CXI +XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XR DXI=DXI +XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI −ZI

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FIG. 78

C4

AWR=AWR +WR AWI=AWI +WI	AXR=AXR −XR AXI=AXI −XI	AYR=AYR +YR AYI=AYI +YI	AZR=AZR −ZR AZI=AZI −ZI
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YR BYI=BYI +YI	BZR=BZR −ZR BZI=BZI −ZI
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YR CYI=CYI +YI	CZR=CZR −ZR CZI=CZI −ZI
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YR DYI=DYI +YI	DZR=DZR −ZR DZI=DZI −ZI

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FIG. 79

C5

AWR=AWR −WI AWI=AWI +WR	AXR=AXR +XI AXI=AXI −XR	AYR=AYR −YI AYI=AYI +YR	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR−WI BWI=BWI +WR	BXR=BXR +XI BXI=BXI −XR	BYR=BYR −YI BYI=BYI +YR	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR−WI CWI=CWI +WR	CXR=CXR +XI CXI=CXI −XR	CYR=CYR −YI CYI=CYI +YR	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR−WI DWI=DWI +WR	DXR=DXR +XI DXI=DXI −XR	DYR=DYR −YI DYI=DYI +YR	DZR=DZR +ZI DZI=DZI −ZR

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FIG. 80

C6

AWR=AWR +WR AWI=AWI +WI	AXR=AXR −XI AXI=AXI +XR	AYR=AYR −YR AYI=AYI −YI	AZR=AZR +ZI AZI=AZI −ZR
BWR=BWR+WR BWI=BWI +WI	BXR=BXR −XI BXI=BXI +XR	BYR=BYR −YR BYI=BYI −YI	BZR=BZR +ZI BZI=BZI −ZR
CWR=CWR+WR CWI=CWI +WI	CXR=CXR −XI CXI=CXI +XR	CYR=CYR −YR CYI=CYI −YI	CZR=CZR +ZI CZI=CZI −ZR
DWR=DWR+WR DWI=DWI +WI	DXR=DXR −XI DXI=DXI +XR	DYR=DYR −YR DYI=DYI −YI	DZR=DZR +ZI DZI=DZI −ZR

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FIG. 81

C7

AWR=AWR −WI AWI=AWI +WR	AXR=AXR −XR AXI=AXI −XI	AYR=AYR +YI AYI=AYI −YR	AZR=AZR −ZR AZI=AZI +ZI
BWR=BWR−WI BWI=BWI +WR	BXR=BXR −XR BXI=BXI −XI	BYR=BYR +YI BYI=BYI −YR	BZR=BZR −ZR BZI=BZI +ZI
CWR=CWR−WI CWI=CWI +WR	CXR=CXR −XR CXI=CXI −XI	CYR=CYR +YI CYI=CYI −YR	CZR=CZR −ZR CZI=CZI +ZI
DWR=DWR−WI DWI=DWI +WR	DXR=DXR −XR DXI=DXI −XI	DYR=DYR +YI DYI=DYI −YR	DZR=DZR −ZR DZI=DZI +ZI

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FIG. 82

SOFTQUAD SCREENSHOT

THIS TABLE SHOWS THE ORDER OF CALCULATION FOR A TRANSPOSED BUTTERFLY:

C0

2632

AWR =WR+XR+YR+ZR AWI =WI+XI+YI+ZI	AXR =WR−XI−YR+ZI AXI =WI+XR−YI−ZR	AYR =WR−XR+YR−ZR AYI =WI−XI+YI−ZI	AZR =WR+XI−YR−ZI AZI =WI−XR−YI+ZR
− −	− −	− −	− −
− −	− −	− −	− −
− −	− −	− −	− −

2810

FIG. 83

C1

2632

AWR =AWR−(WI+XI+YI+ZI) AWI =AWI+(WR+XR+YR+ZR)	AXR =AXR−(WI+XR−YI−ZR) AXI =AXI+(WR−XI−YR+ZI)	AYR =AYR−(WI−XI+YI−ZI) AYI =AYI+(WR−XR+YR−ZR)	AZR =AZR−(WI−XR−YI+ZR) AZI =AZI+(WR+XI−YR−ZI)
− −	− −	− −	− −
− −	− −	− −	− −
− −	− −	− −	− −

2810

FIG. 84

C2

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2810

– –	– –	– –	– –
BWR =WR+XR+YR+ZR BWI =WI+XI+YI+ZI	BXR =WR−XI−YR+ZI BXI =WI+XR−YI−ZR	BYR =WR−XR+YR−ZR BYI =WI−XI+YI−ZI	BZR =WR+XI−YR−ZI BZI =WI−XR−YI+ZR
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 85

C3

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2810

– –	– –	– –	– –
BWR =BWR−(WI+XI+YI+ZI) BWI =BWI+(WR+XR+YR+ZR)	BXR =BXR−(WI+XR−YI−ZR) BXI =BXI+(WR−XI−YR+ZI)	BYR =BYR−(WI−XI+YI−ZI) BYI =BYI+(WR−XR+YR−ZR)	BZR =BZR−(WI−XR−YI+ZR) BZI =BZI+(WR+XI−YR−ZI)
– –	– –	– –	– –
– –	– –	– –	– –

FIG. 86

DRAFT - DO NOT SCAN

C4

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–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
CWR =WR+XR+YR+ZR CWI =WI+XI+YI+ZI	CXR =WR−XI−YR+ZI CXI =WI+XR−YI−ZR	CYR =WR−XR+YR−ZR CYI =WI−XI+YI−ZI	CZR =WR+XI−YR−ZI CZI =WI−XR−YI+ZR
–	–	–	–
–	–	–	–

FIG. 87

C5

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–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
CWR =CWR−(WI+XI+YI+ZI) CWI =CWI+(WR+XR+YR+ZR)	CXR =CXR−(WI+XR−YI−ZR) CXI =CXI+(WR−XI−YR+ZI)	CYR =CYR−(WI−XI+YI−ZI) CYI =CYI+(WR−XR+YR−ZR)	CZR =CZR−(WI−XR−YI+ZR) CZI =CZI+(WR+XI−YR−ZI)
–	–	–	–
–	–	–	–

FIG. 88

C6

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–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
DWR =WR+XR+YR+ZR DWI =WI+XI+YI+ZI	DXR =WR−XI−YR+ZI DXI =WI+XR−YI−ZR	DYR =WR−XR+YR−ZR DYI =WI−XI+YI−ZI	DZR =WR+XI−YR−ZI DZI =WI−XR−YI+ZR

FIG. 89

C7

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–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–
DWR =DWR−(WI+XI+YI+ZI) DWI =DWI+(WR+XR+YR+ZR)	DXR =DXR−(WI+XR−YI−ZR) DXI =DXI+(WR−XI−YR+ZI)	DYR =DYR−(WI−XI+YI−ZI) DYI =DYI+(WR−XR+YR−ZR)	DZR =DZR−(WI−XR−YI+ZR) DZI =DZI+(WR+XI−YR−ZI)

FIG. 90

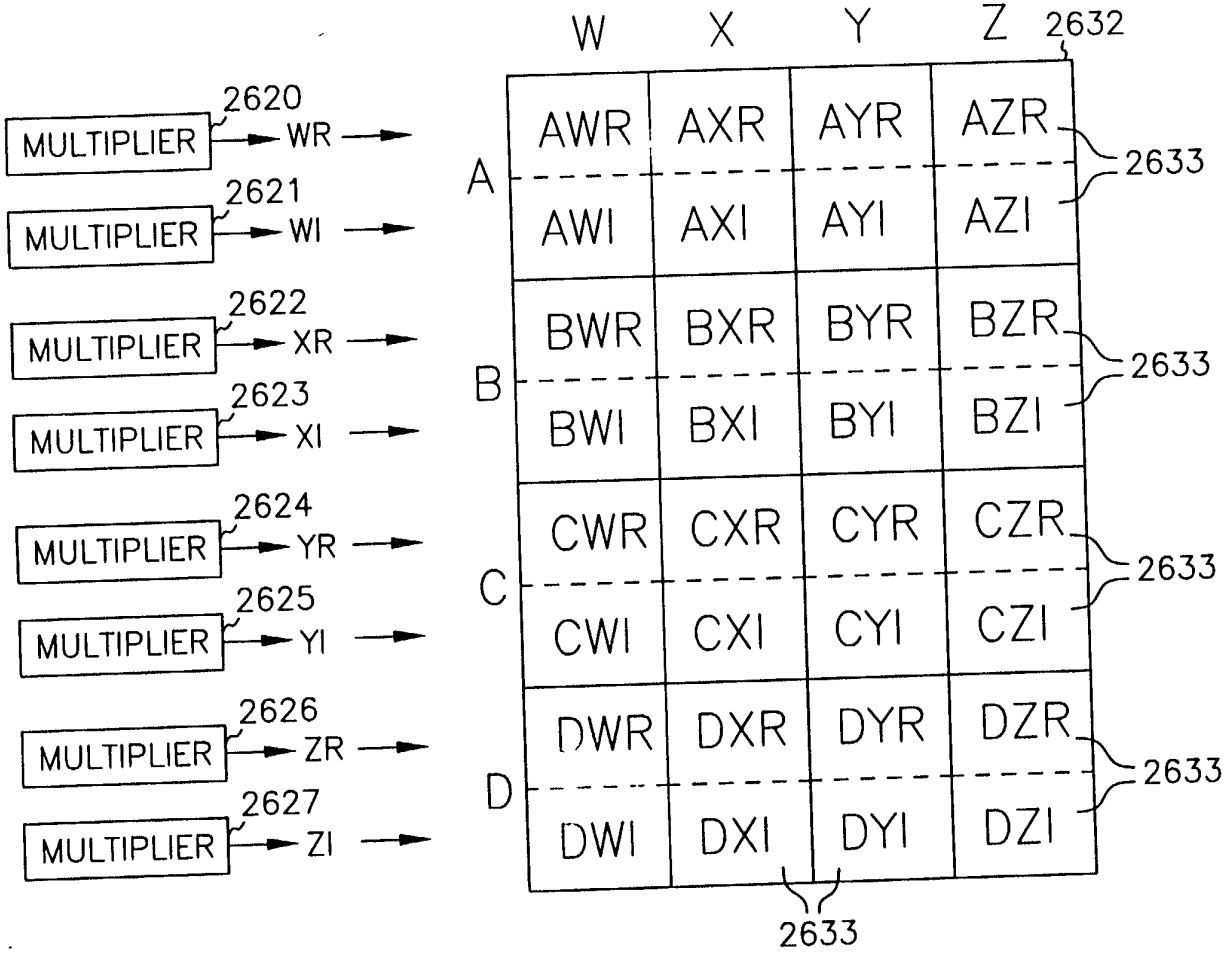

MULTIPLIER
2620
WR
MULTIPLIER
2621
WI
MULTIPLIER
2622
XR
MULTIPLIER
2623
XI
MULTIPLIER
2624
YR
MULTIPLIER
2625
YI
MULTIPLIER
2626
ZR
MULTIPLIER
2627
ZI
W
X
Y
Z
2632
A
B
C
D
AWR
AXR
AYR
AZR
AWI
AXI
AYI
AZI
BWR
BXR
BYR
BZR
BWI
BXI
BYI
BZI
CWR
CXR
CYR
CZR
CWI
CXI
CYI
CZI
DWR
DXR
DYR
DZR
DWI
DXI
DYI
DZI
2633
2633
2633
2633
2633

FIG. 91

20FT0 ES2ch0t

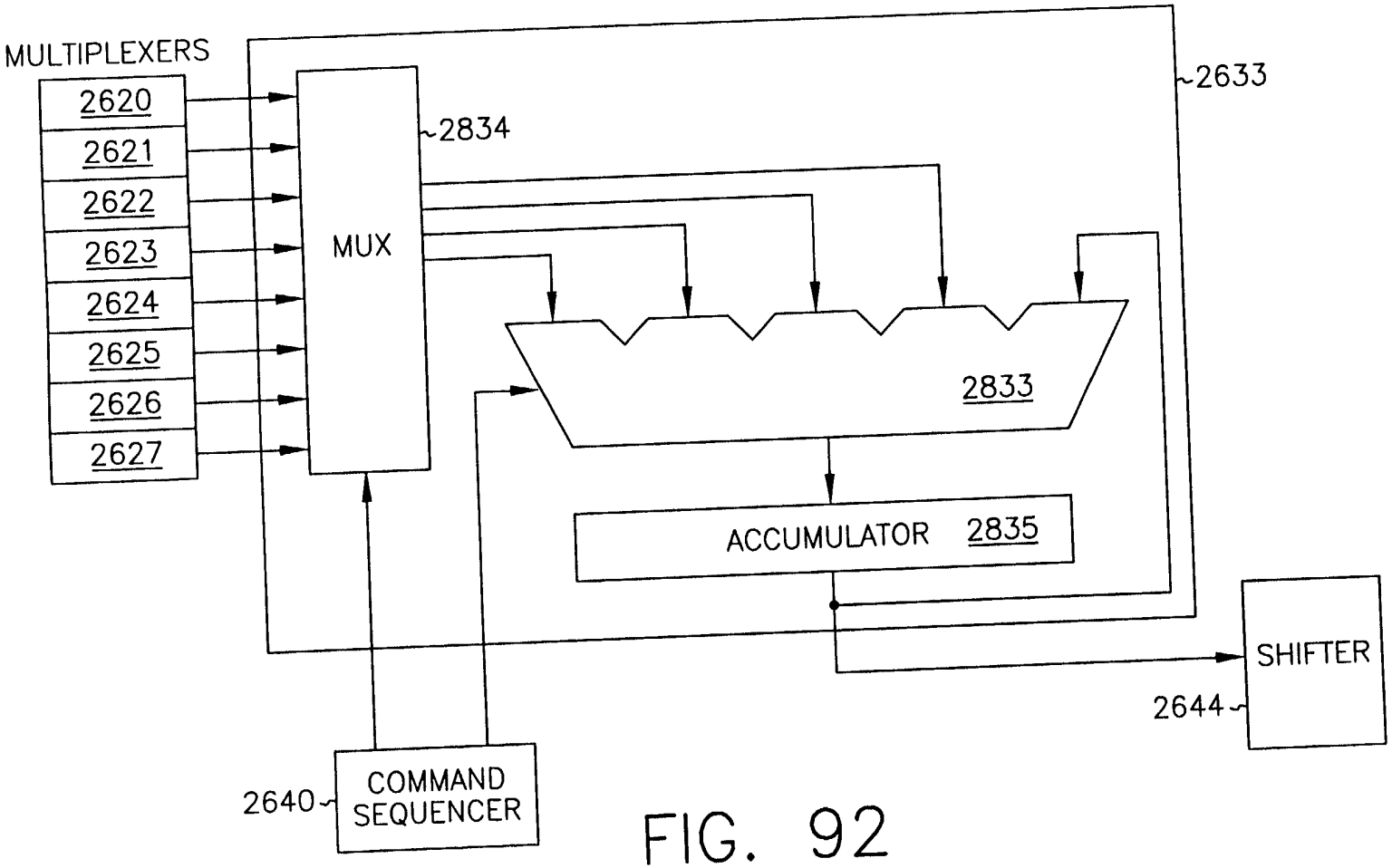


FIG. 92

Patent Search

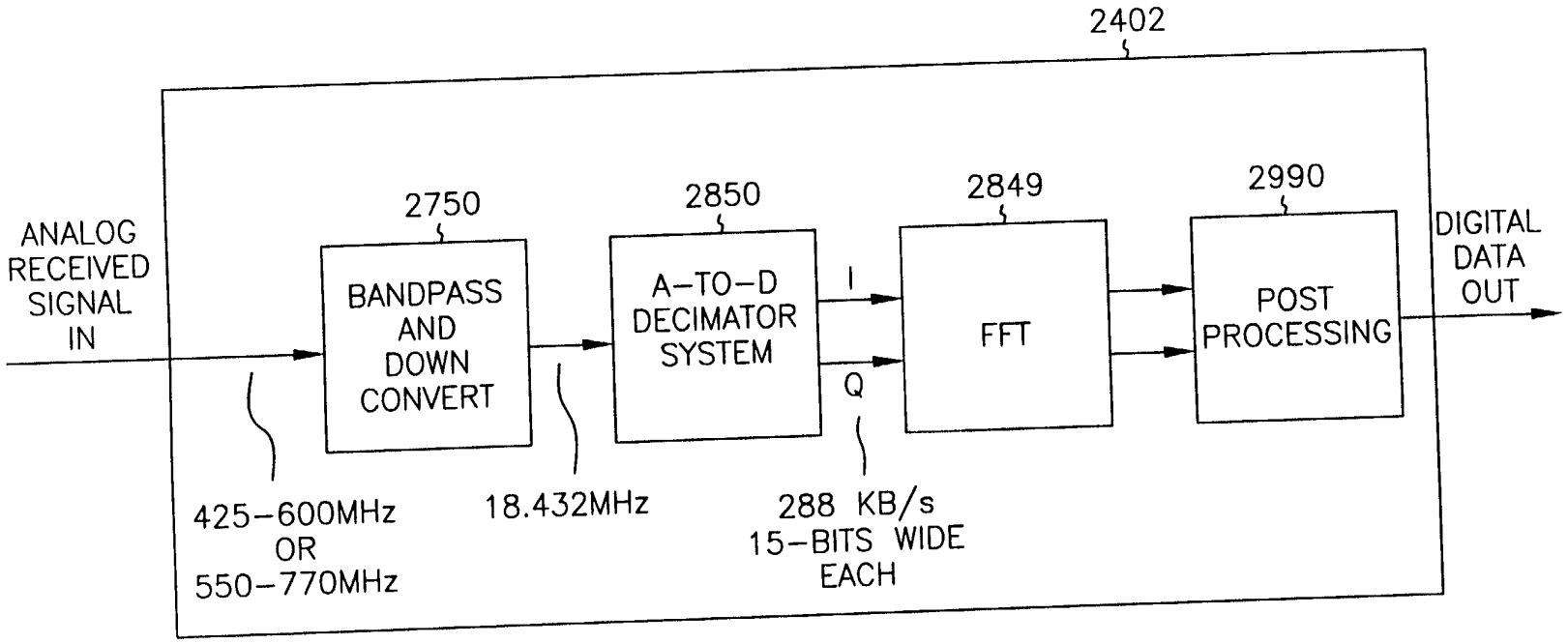


FIG. 93

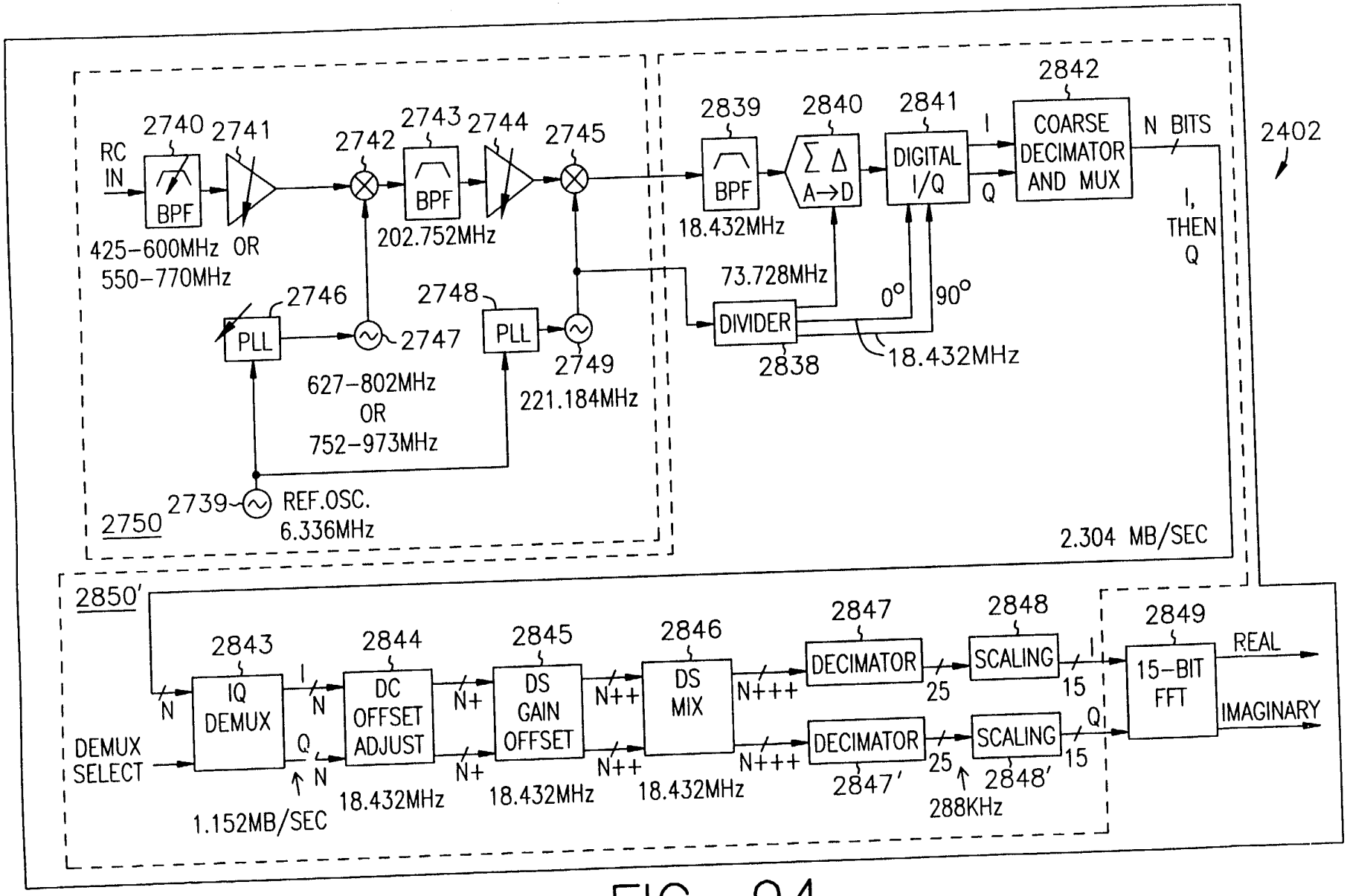

2402
RC IN
2740
BPF
425–600MHz OR
550–770MHz
2741
2742
2743
BPF
202.752MHz
2744
2745
2746
PLL
2747
627–802MHz
OR
752–973MHz
2748
PLL
2749
221.184MHz
2739
REF.OSC.
6.336MHz
2750
2839
BPF
18.432MHz
2840
Σ Δ
A→D
2841
DIGITAL
I/Q
I
Q
2842
COARSE
DECIMATOR
AND MUX
N BITS
I,
THEN
Q
2.304 MB/SEC
73.728MHz
DIVIDER
2838
0°
90°
18.432MHz
2850'
2843
IQ
DEMUX
N
I
Q
N
DEMUX
SELECT
1.152MB/SEC
2844
DC
OFFSET
ADJUST
18.432MHz
N+
N+
2845
DS
GAIN
OFFSET
18.432MHz
N++
N++
2846
DS
MIX
18.432MHz
N+++
N+++
2847
DECIMATOR
25
2847'
DECIMATOR
25
2848
SCALING
15
I
2848'
SCALING
15
Q
288KHz
2849
15-BIT
FFT
REAL
IMAGINARY

FIG. 94

SUBSTITUTE SHEET

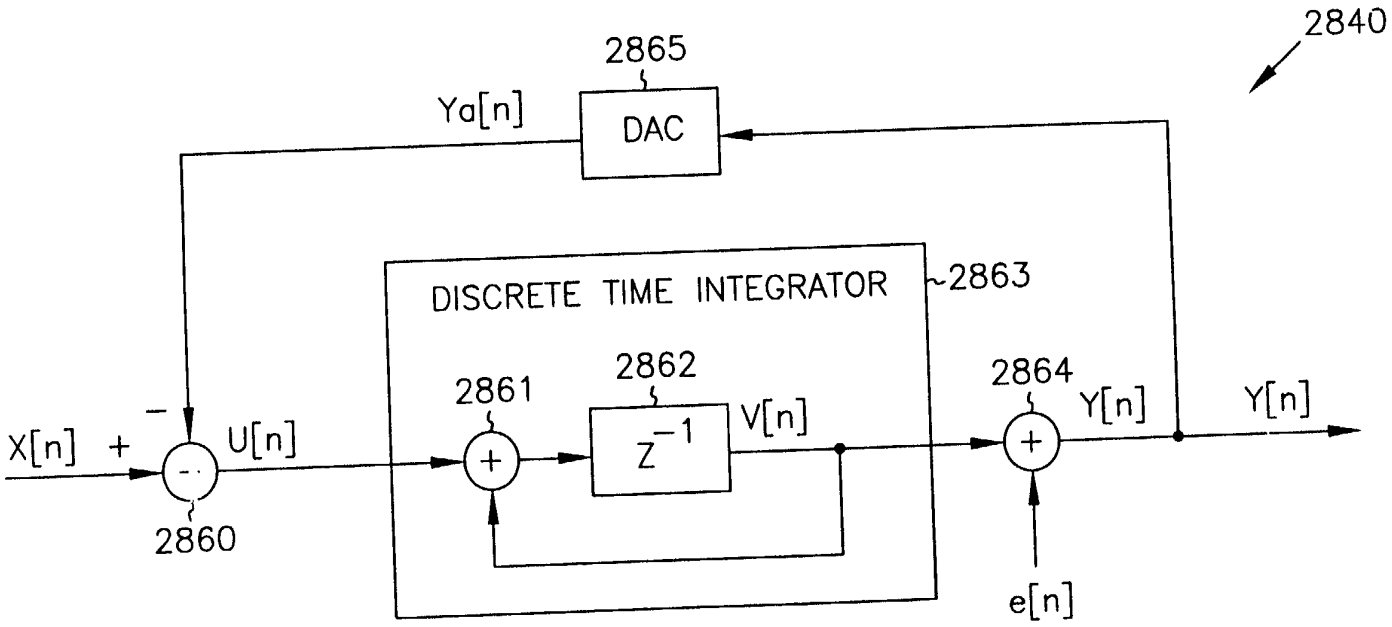


FIG. 95

patent search

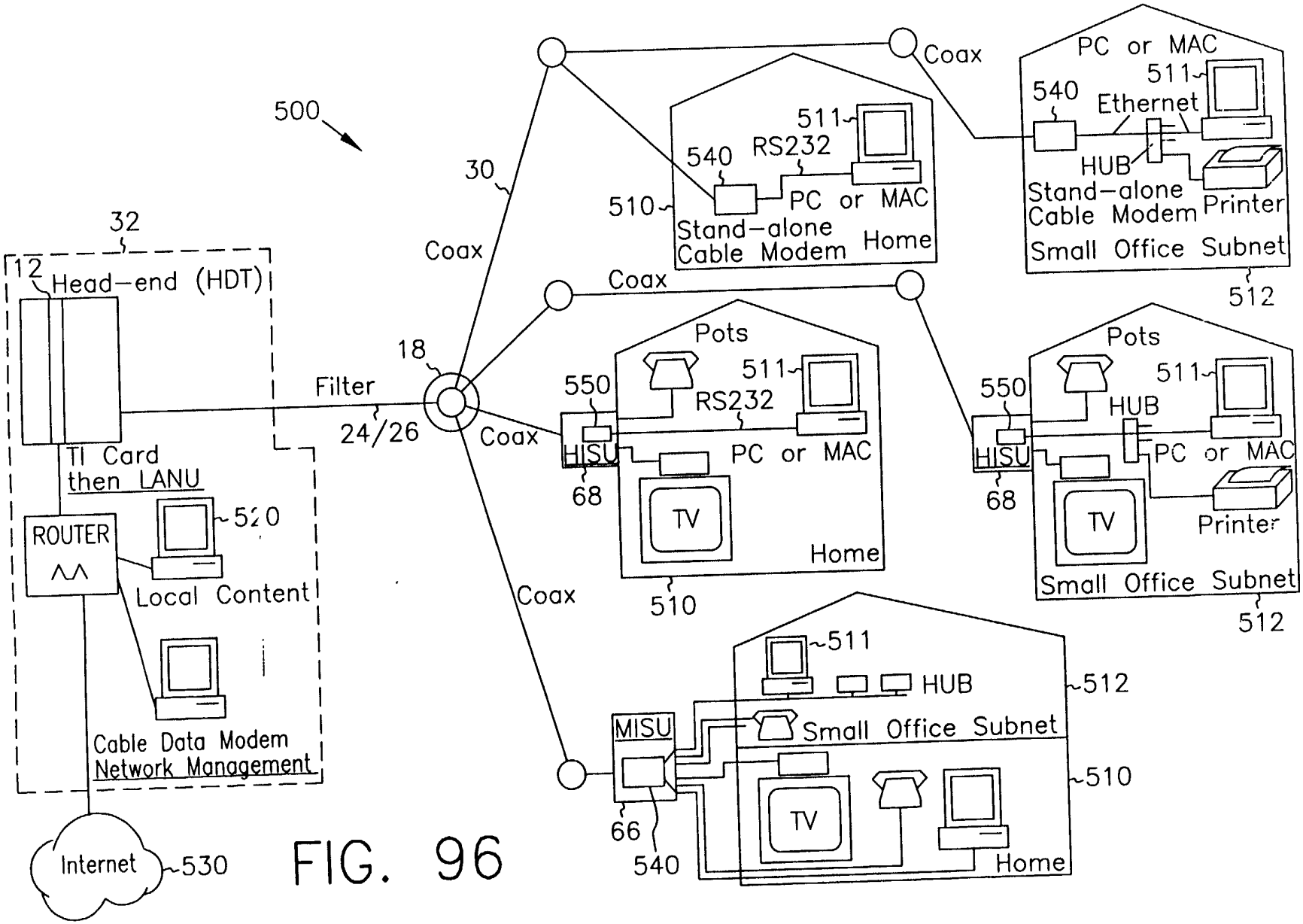


FIG. 96

PATENT SEARCH

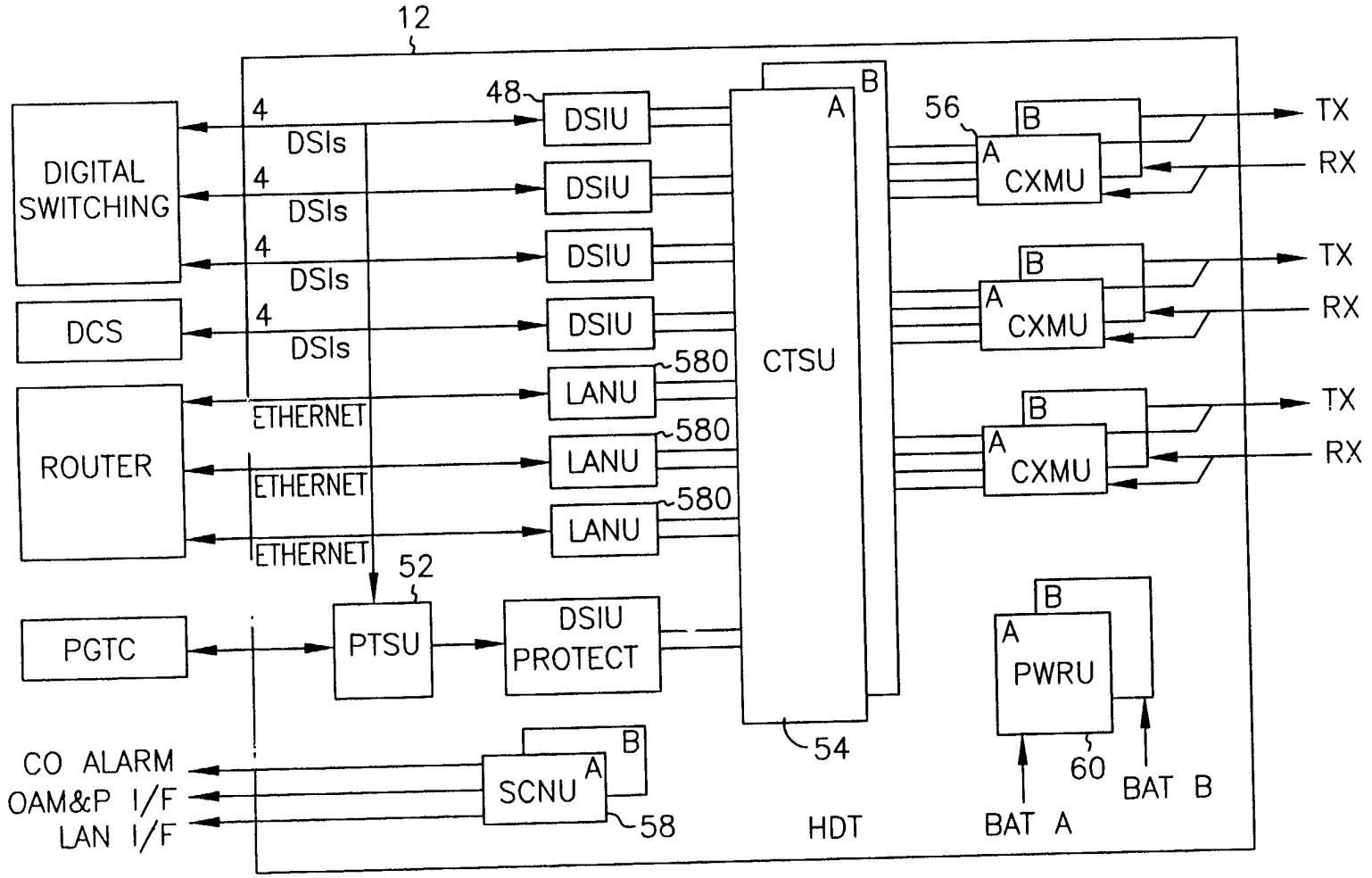


FIG. 97

20FT0 ES2ETH07

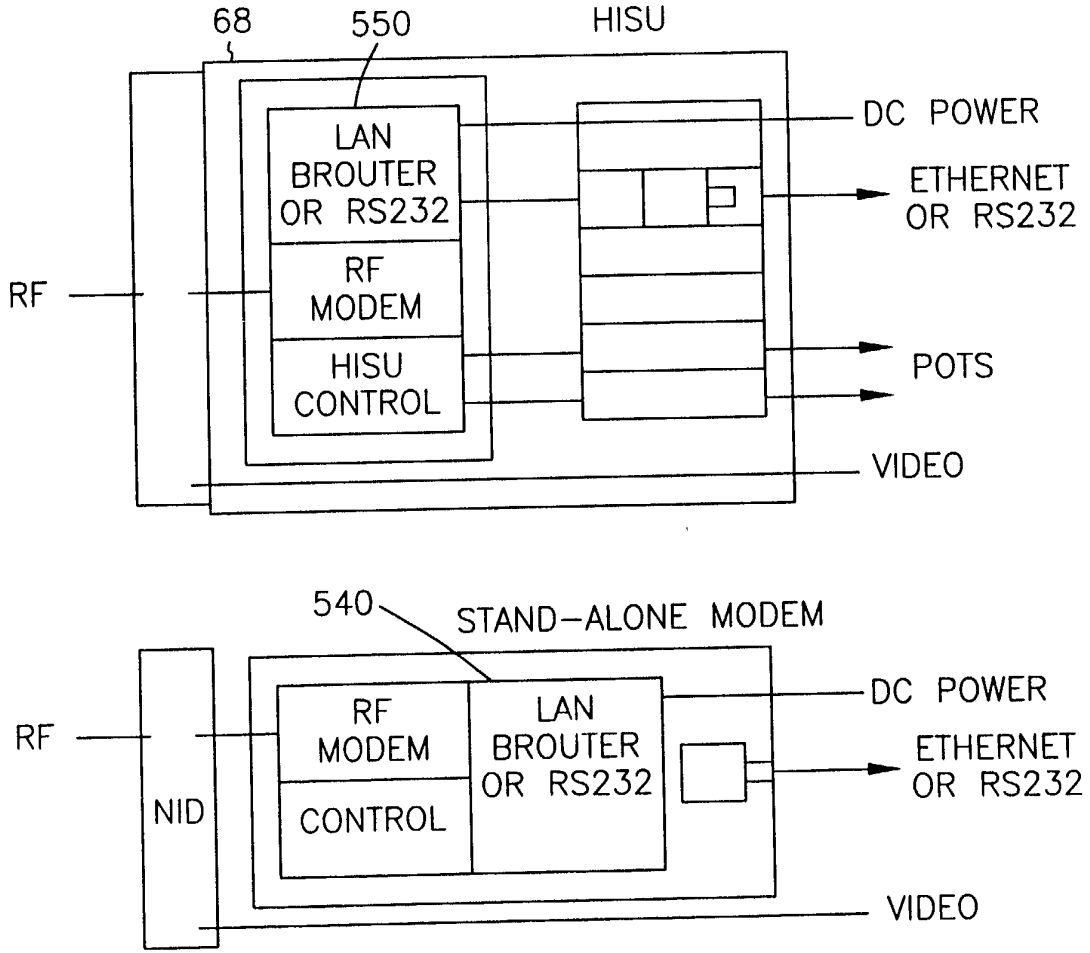


FIG. 98

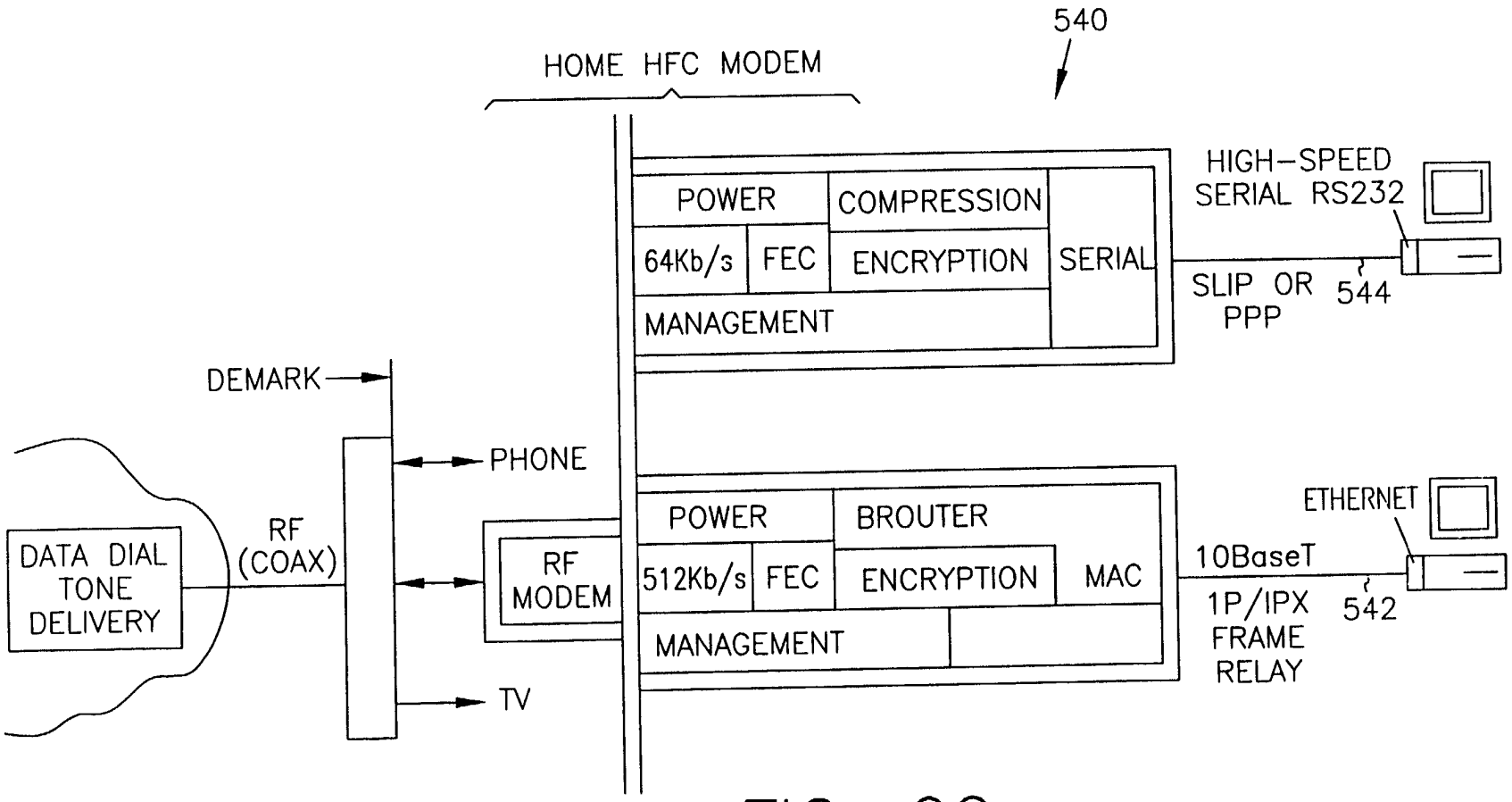

540
HOME HFC MODEM
POWER
COMPRESSION
64Kb/s
FEC
ENCRYPTION
SERIAL
MANAGEMENT
HIGH-SPEED SERIAL RS232
SLIP OR PPP
544
DEMARK
PHONE
DATA DIAL TONE DELIVERY
RF (COAX)
RF MODEM
POWER
BROUTER
512Kb/s
FEC
ENCRYPTION
MAC
MANAGEMENT
ETHERNET
10BaseT
1P/IPX FRAME RELAY
542
TV

FIG. 99

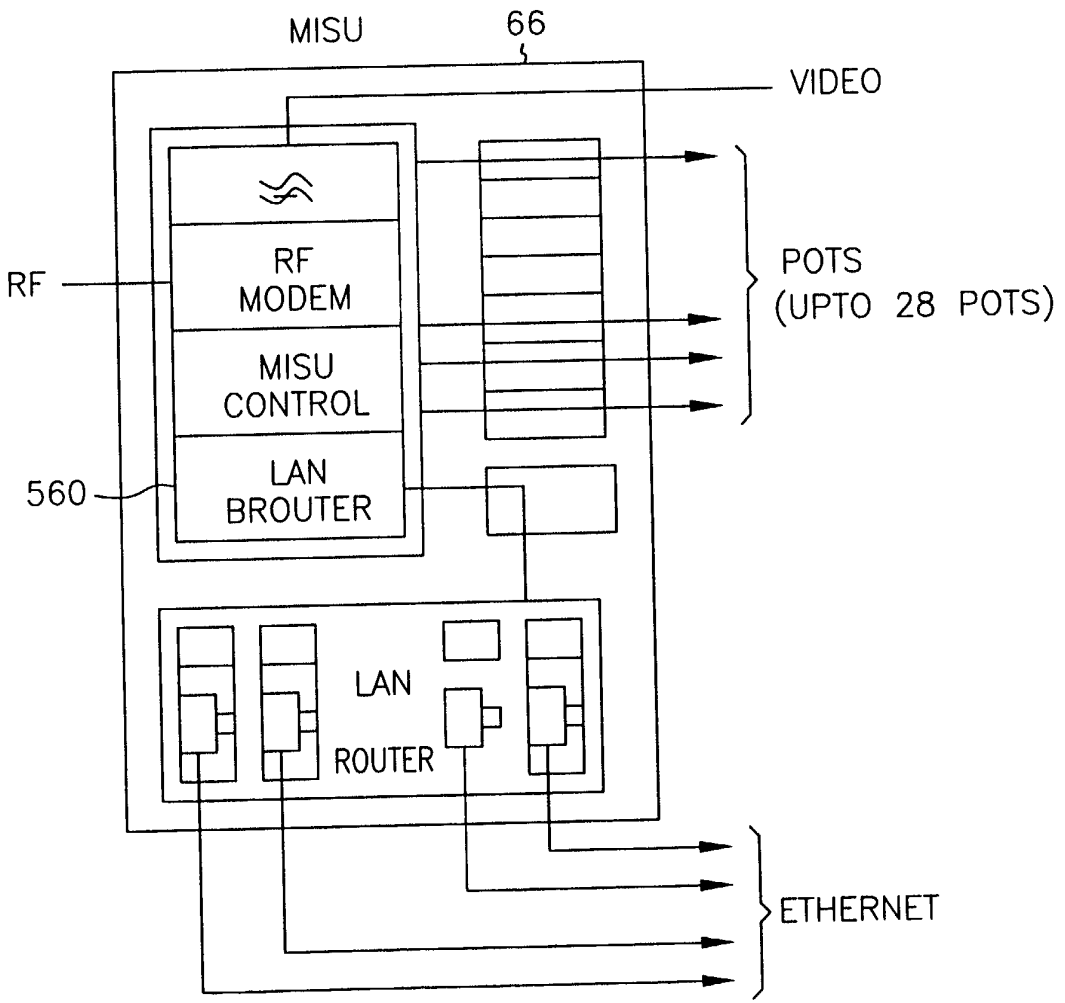

MISU
66
VIDEO
RF
RF MODEM
MISU CONTROL
LAN BROUTER
560
POTS
(UPTO 28 POTS)
LAN
ROUTER
ETHERNET

FIG. 100

EPO - DG 2

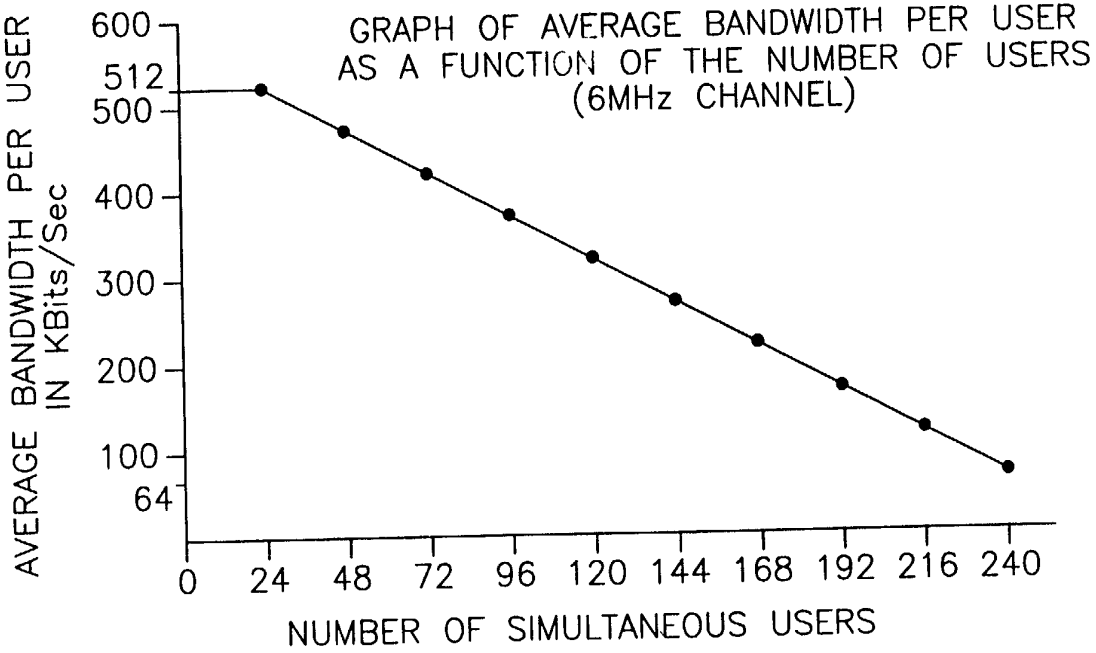


FIG. 101

Patent Research

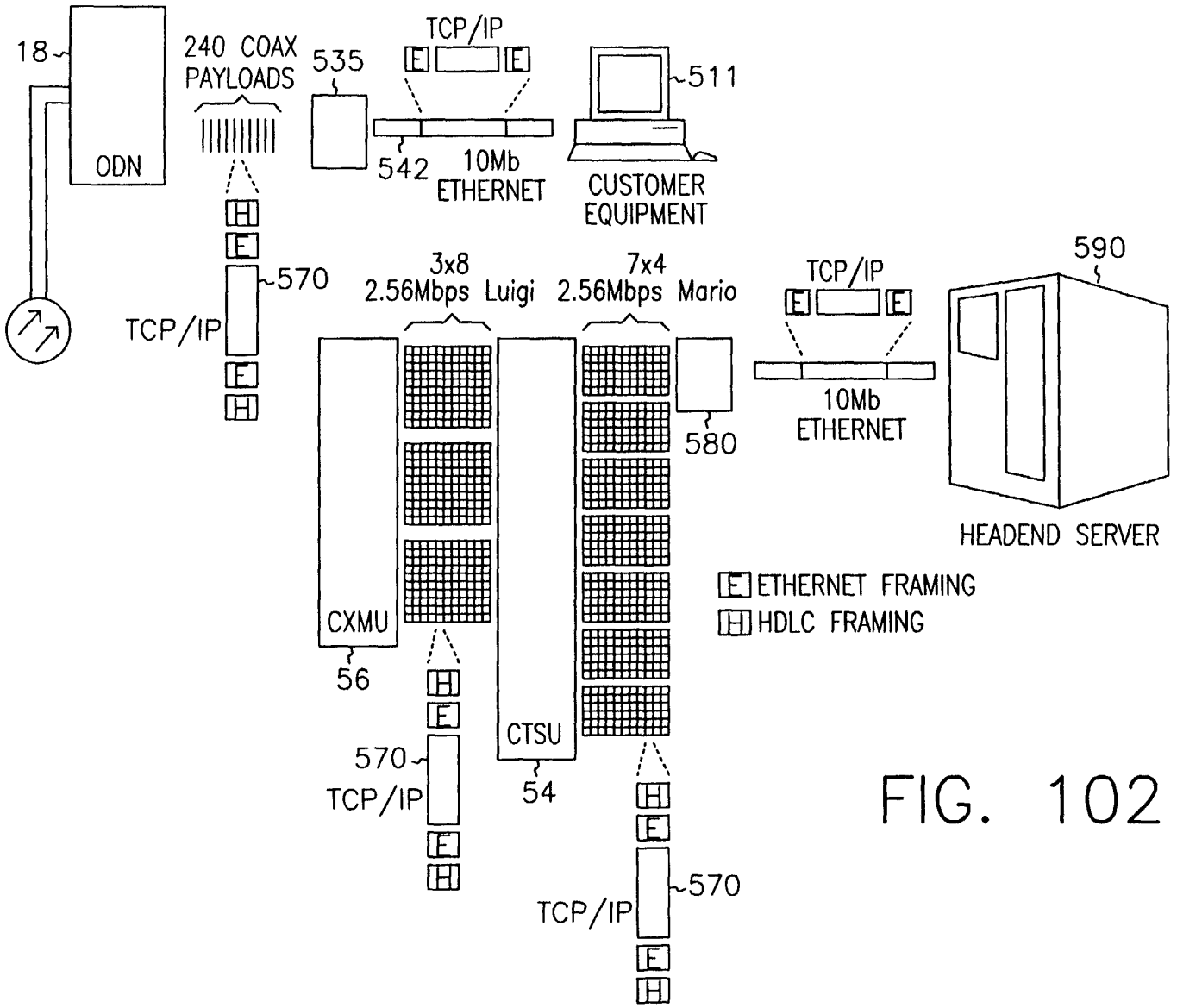


FIG. 102

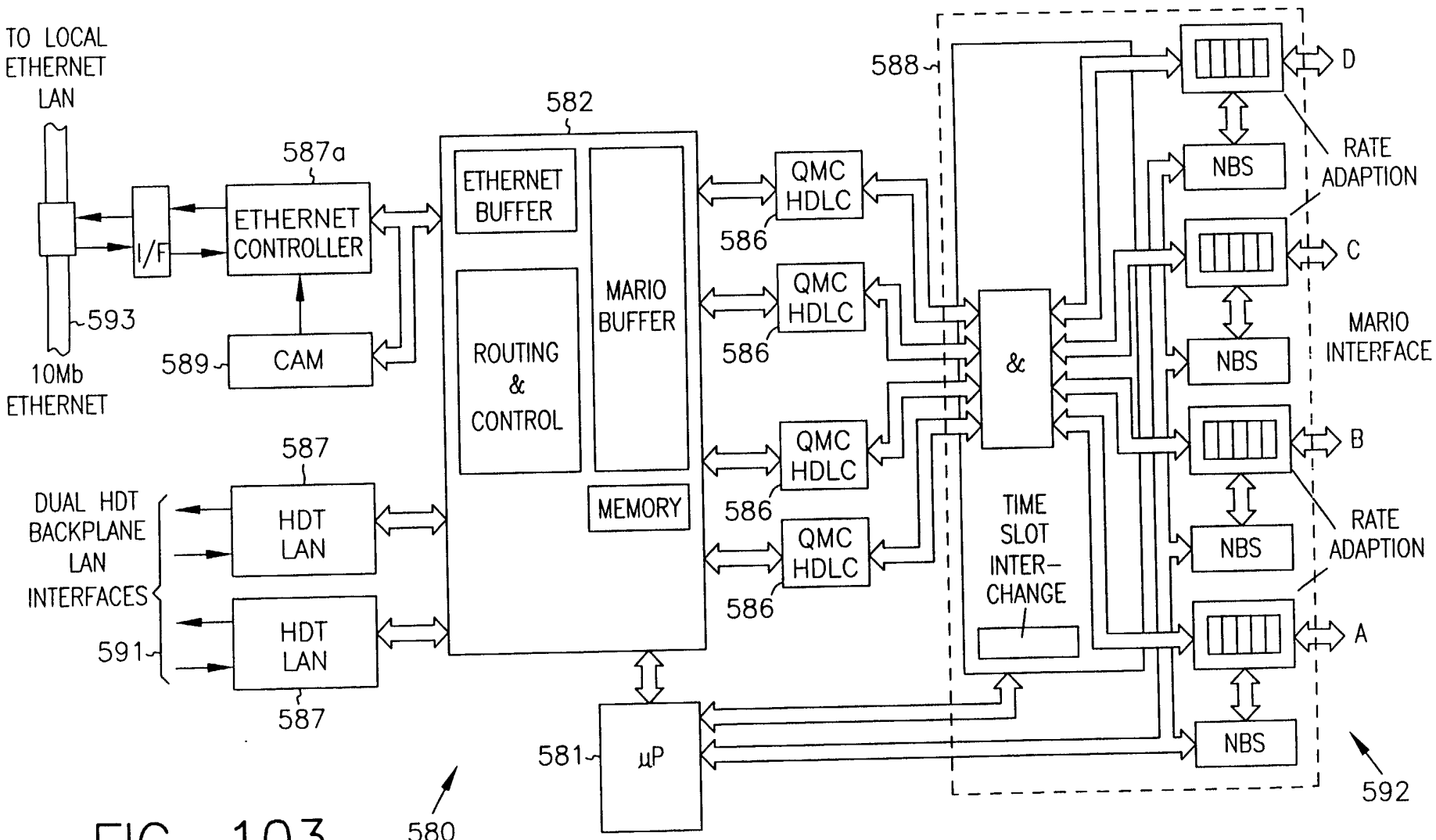

TO LOCAL ETHERNET LAN
10Mb ETHERNET
593
I/F
587a
ETHERNET CONTROLLER
589
CAM
582
ETHERNET BUFFER
ROUTING & CONTROL
MARIO BUFFER
MEMORY
587
DUAL HDT BACKPLANE LAN INTERFACES
591
HDT LAN
HDT LAN
587
581
µP
580
QMC HDLC
QMC HDLC
QMC HDLC
QMC HDLC
586
586
586
586
588
&
TIME SLOT INTER-CHANGE
NBS
NBS
NBS
NBS
RATE ADAPTION
RATE ADAPTION
MARIO INTERFACE
D
C
B
A
592

FIG. 103

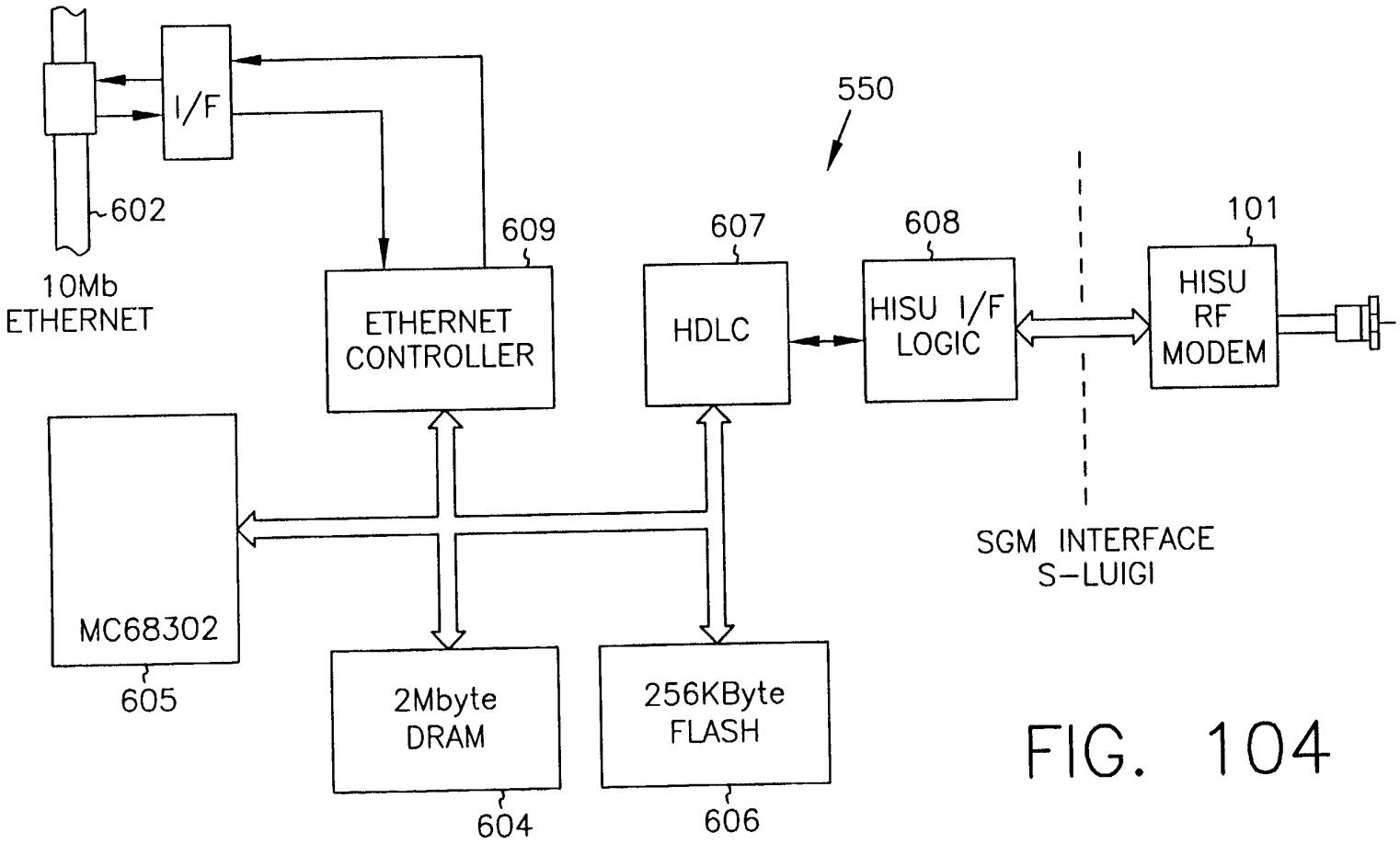

I/F
602
10Mb
ETHERNET
609
ETHERNET
CONTROLLER
550
607
HDLC
608
HISU I/F
LOGIC
101
HISU
RF
MODEM
SGM INTERFACE
S-LUIGI
MC68302
605
2Mbyte
DRAM
604
256KByte
FLASH
606

FIG. 104

20TTD ES2ch00T

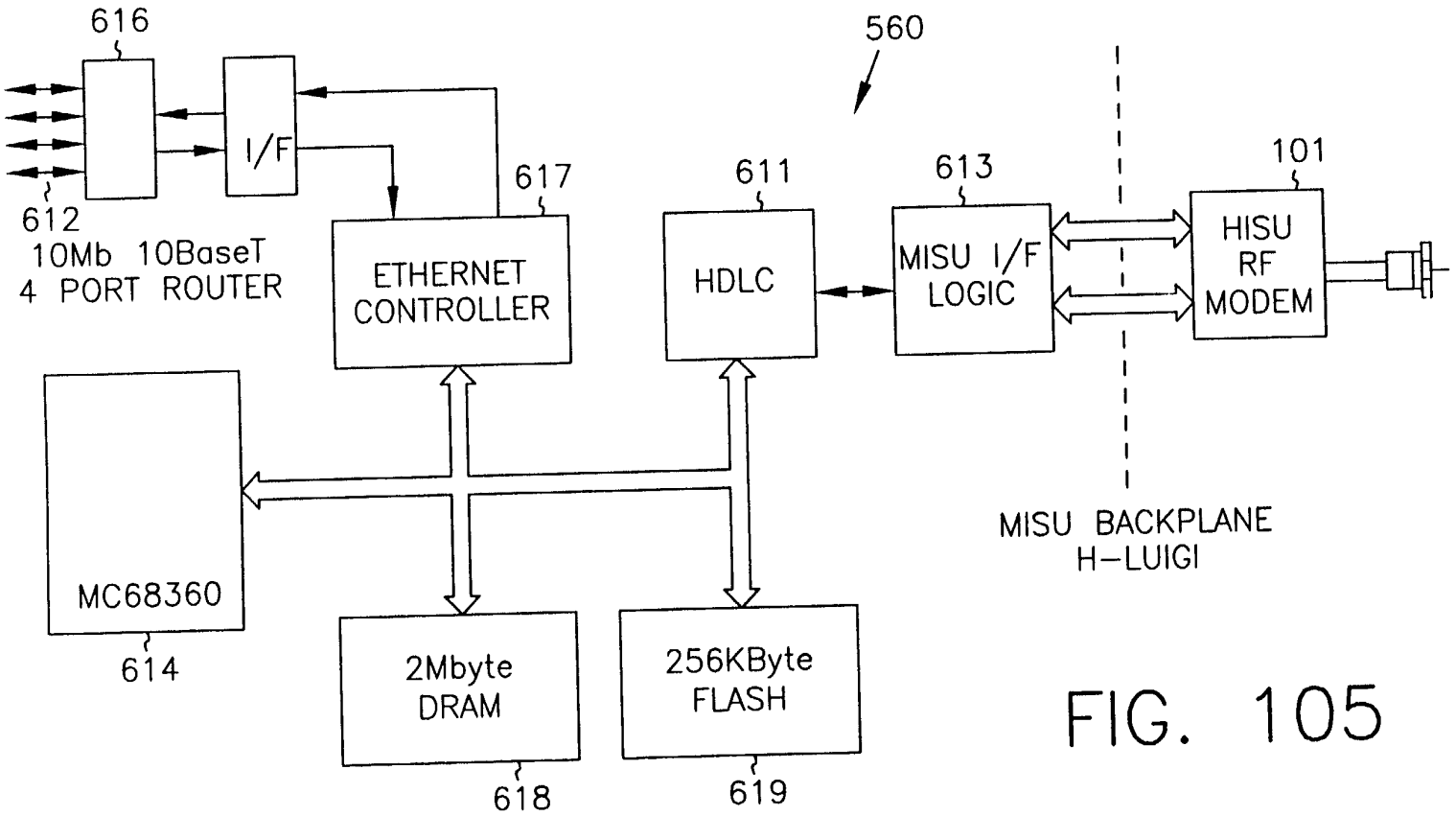


FIG. 105

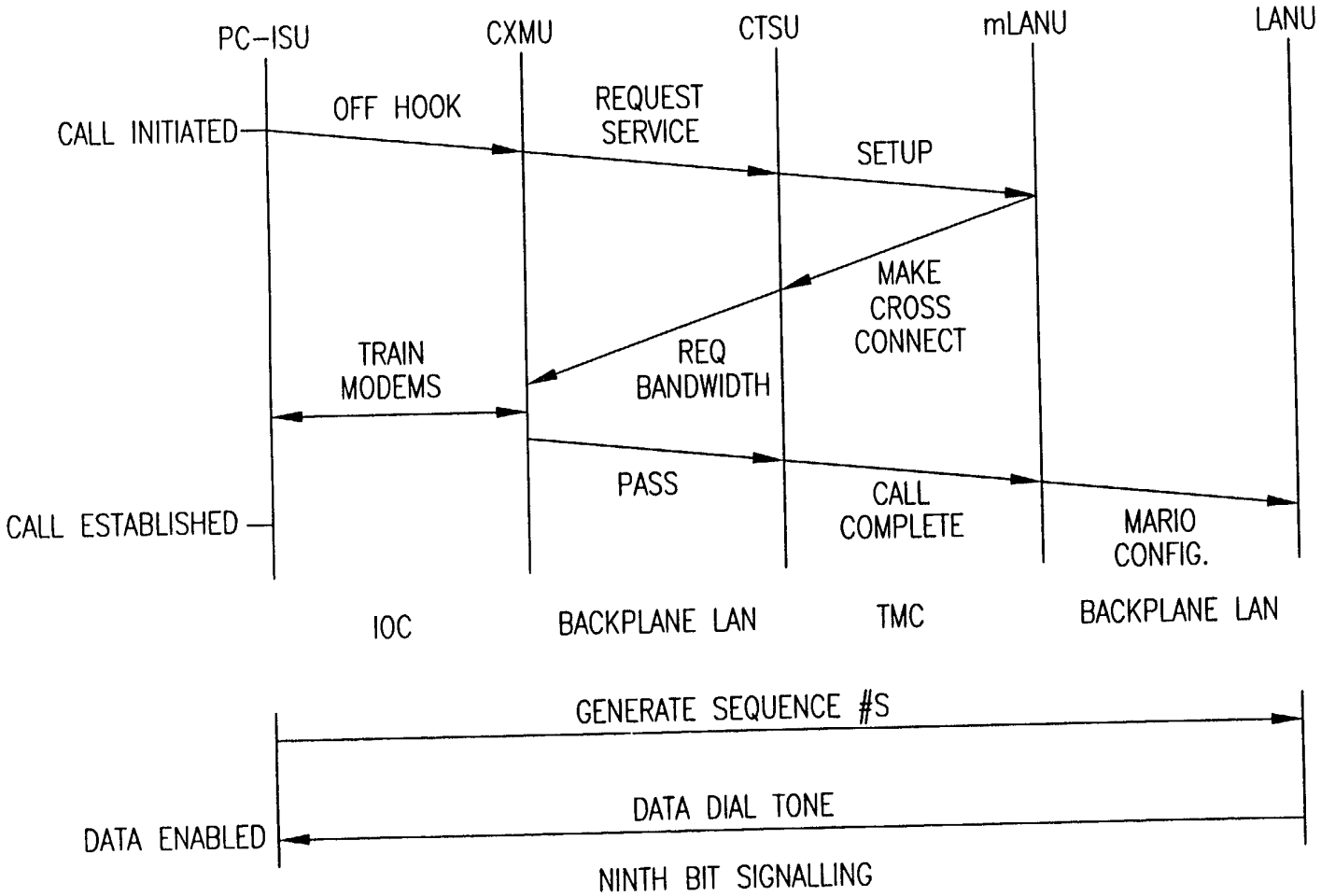

PC-ISU
CXMU
CTSU
mLANU
LANU
CALL INITIATED
OFF HOOK
REQUEST SERVICE
SETUP
MAKE CROSS CONNECT
TRAIN MODEMS
REQ BANDWIDTH
PASS
CALL COMPLETE
MARIO CONFIG.
CALL ESTABLISHED
IOC
BACKPLANE LAN
TMC
BACKPLANE LAN
GENERATE SEQUENCE #S
DATA DIAL TONE
DATA ENABLED
NINTH BIT SIGNALLING

FIG. 106

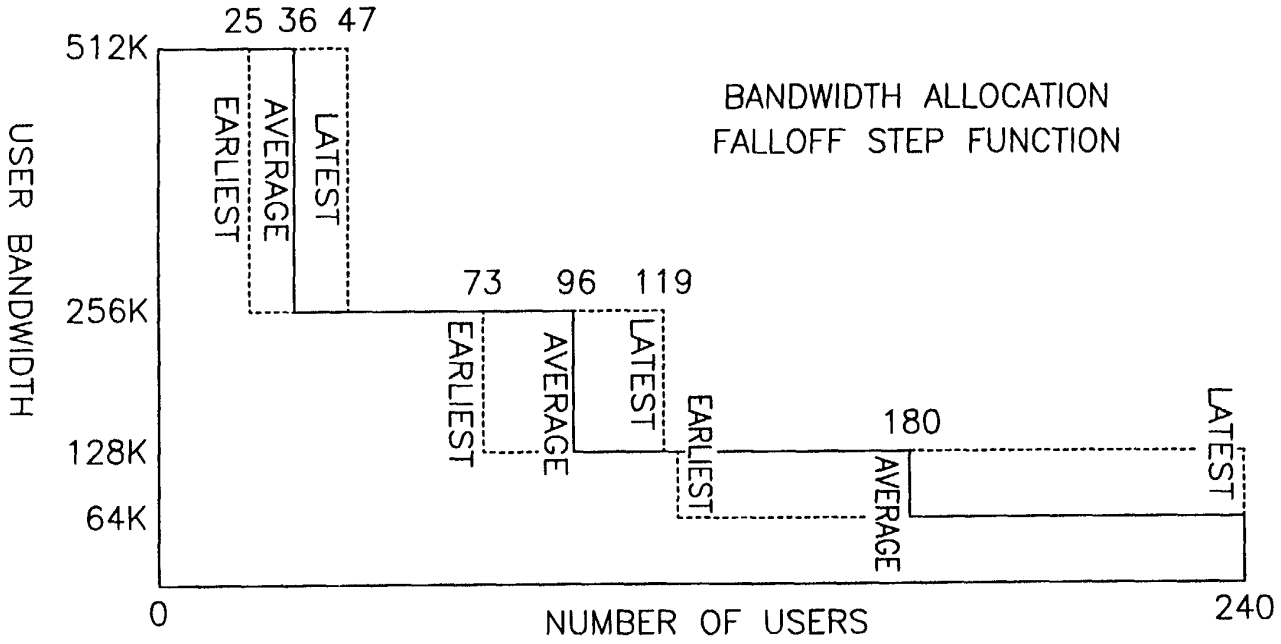
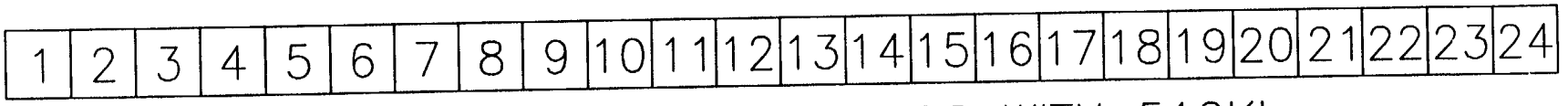
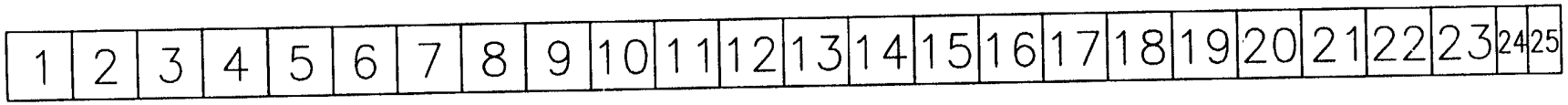

BANDWIDTH ALLOCATION
FALLOFF STEP FUNCTION
USER BANDWIDTH
512K
256K
128K
64K
0
25 36 47
73 96 119
180
EARLIEST
AVERAGE
LATEST
NUMBER OF USERS
240

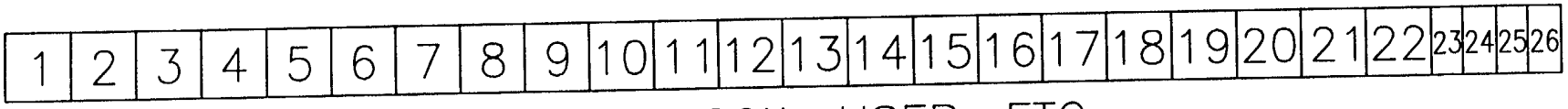
FIG. 107



THE RF SPECTRUM OF 24 USERS WITH 512Kbs



ADDING THE 25th USER



ADDING THE 26th USER, ETC

FIG. 108

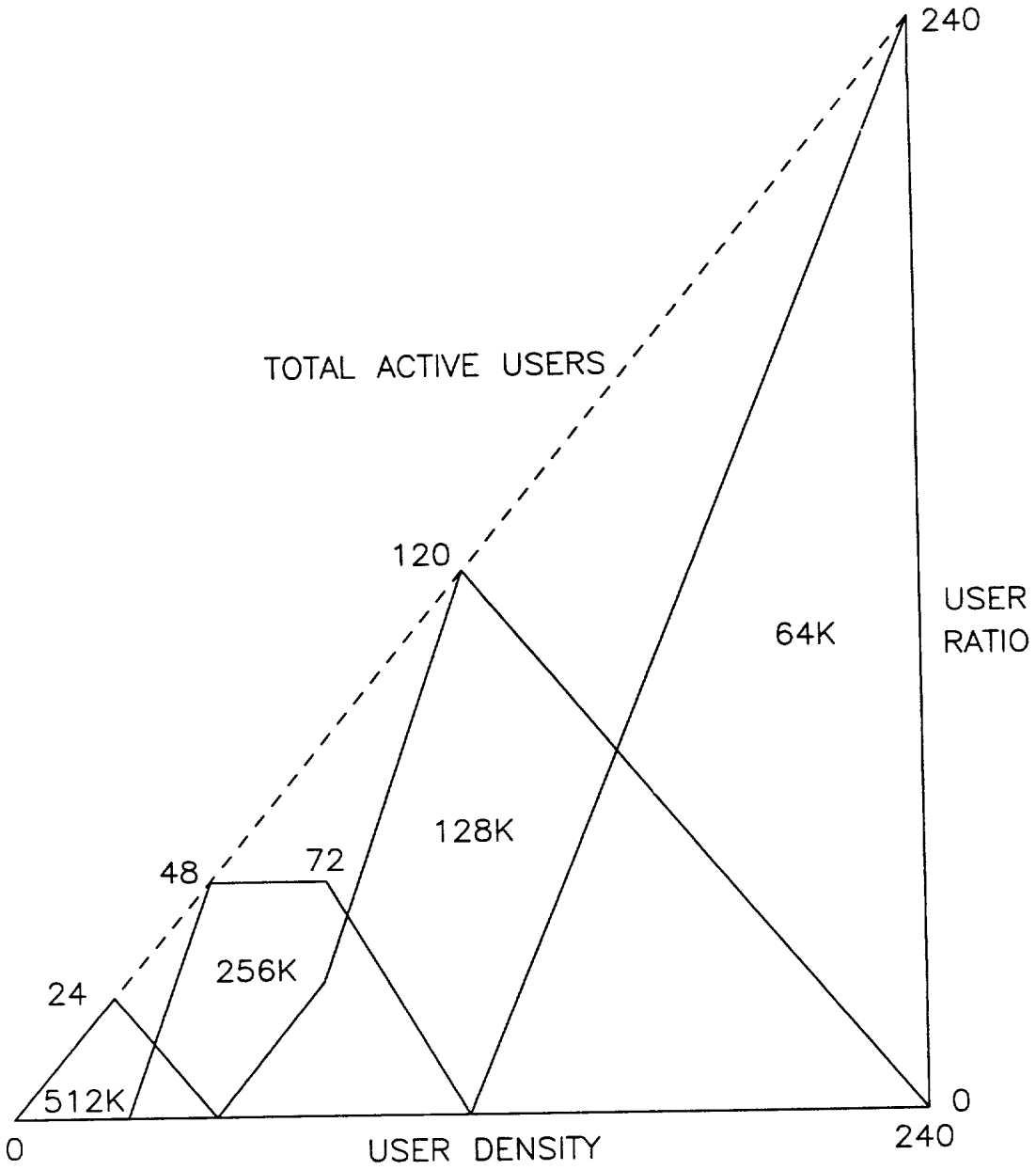

240
TOTAL ACTIVE USERS
120
USER
RATIO
64K
128K
48
72
256K
24
512K
0
0
USER DENSITY
240

FIG. 109

Softto Esz Enoot

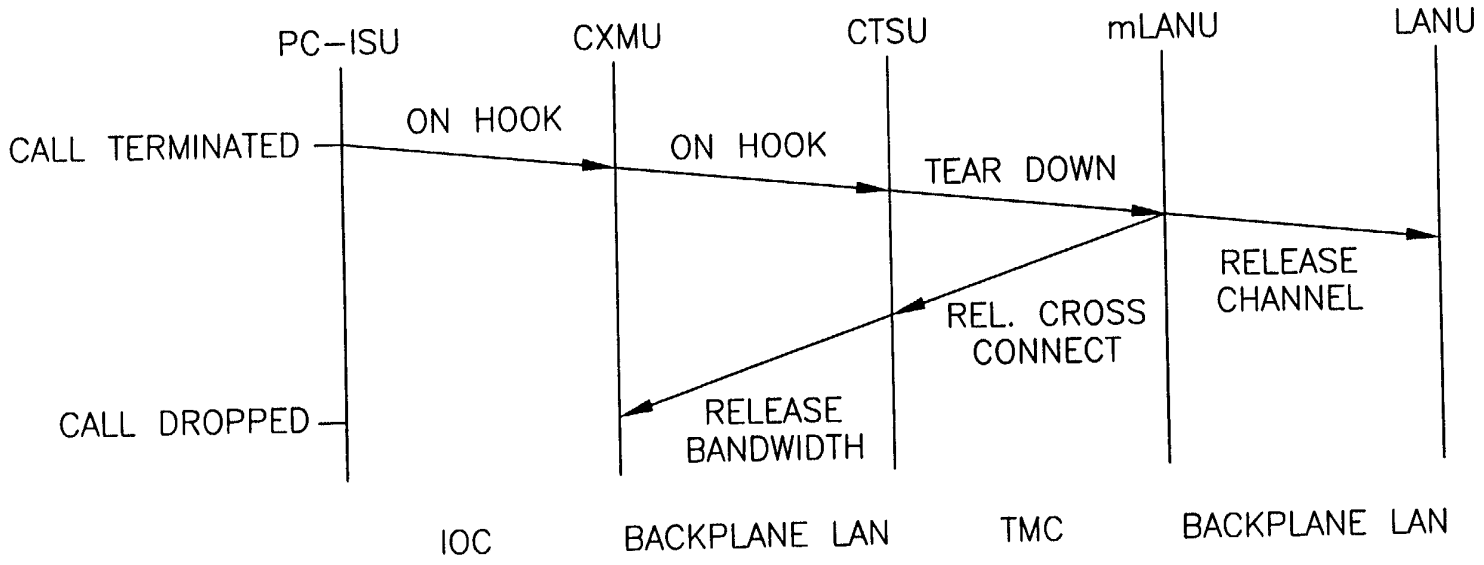


FIG. 110

2017-10-25 21:26:08

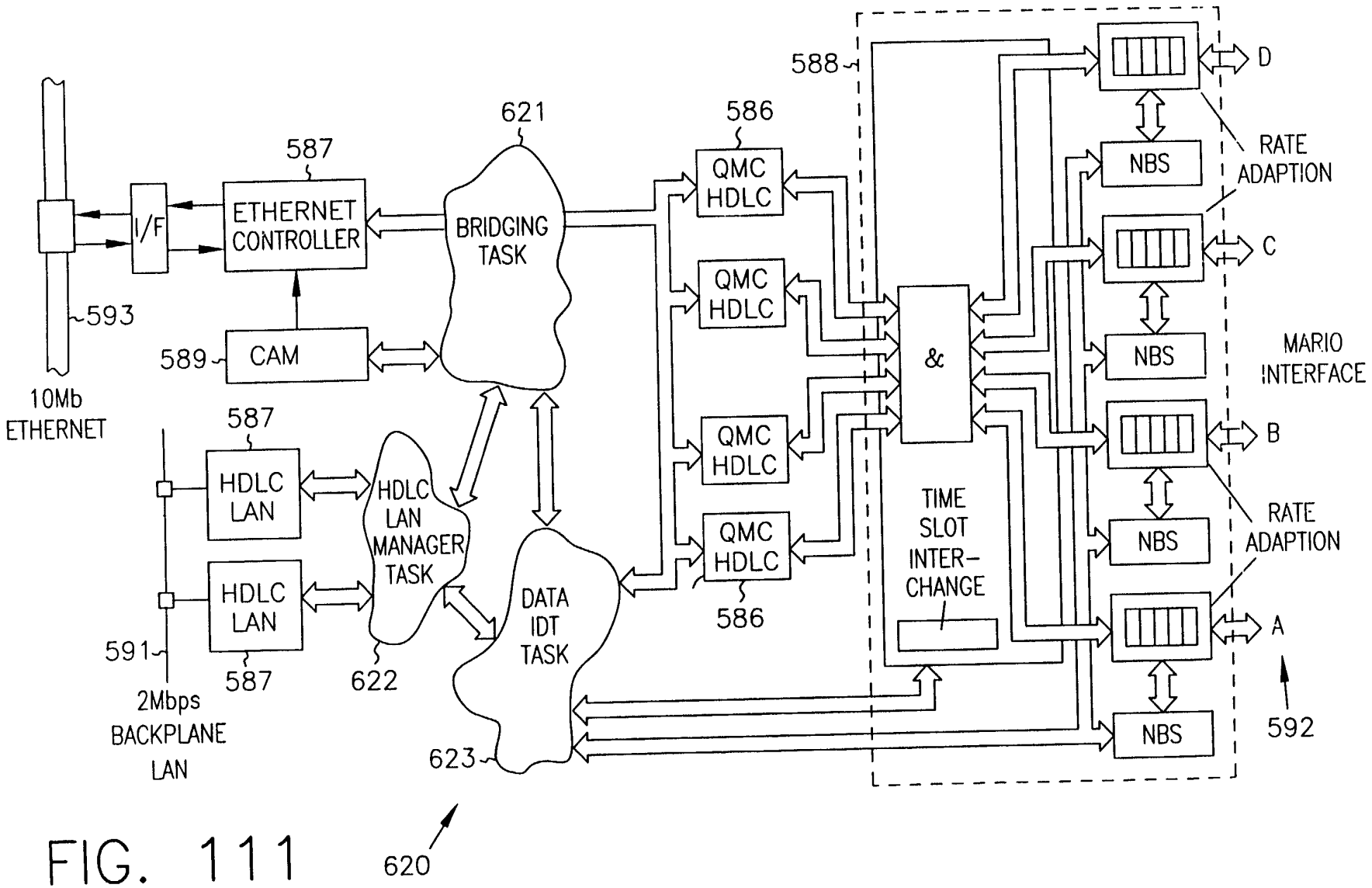


FIG. 111

DRAFT - 2002-08-07

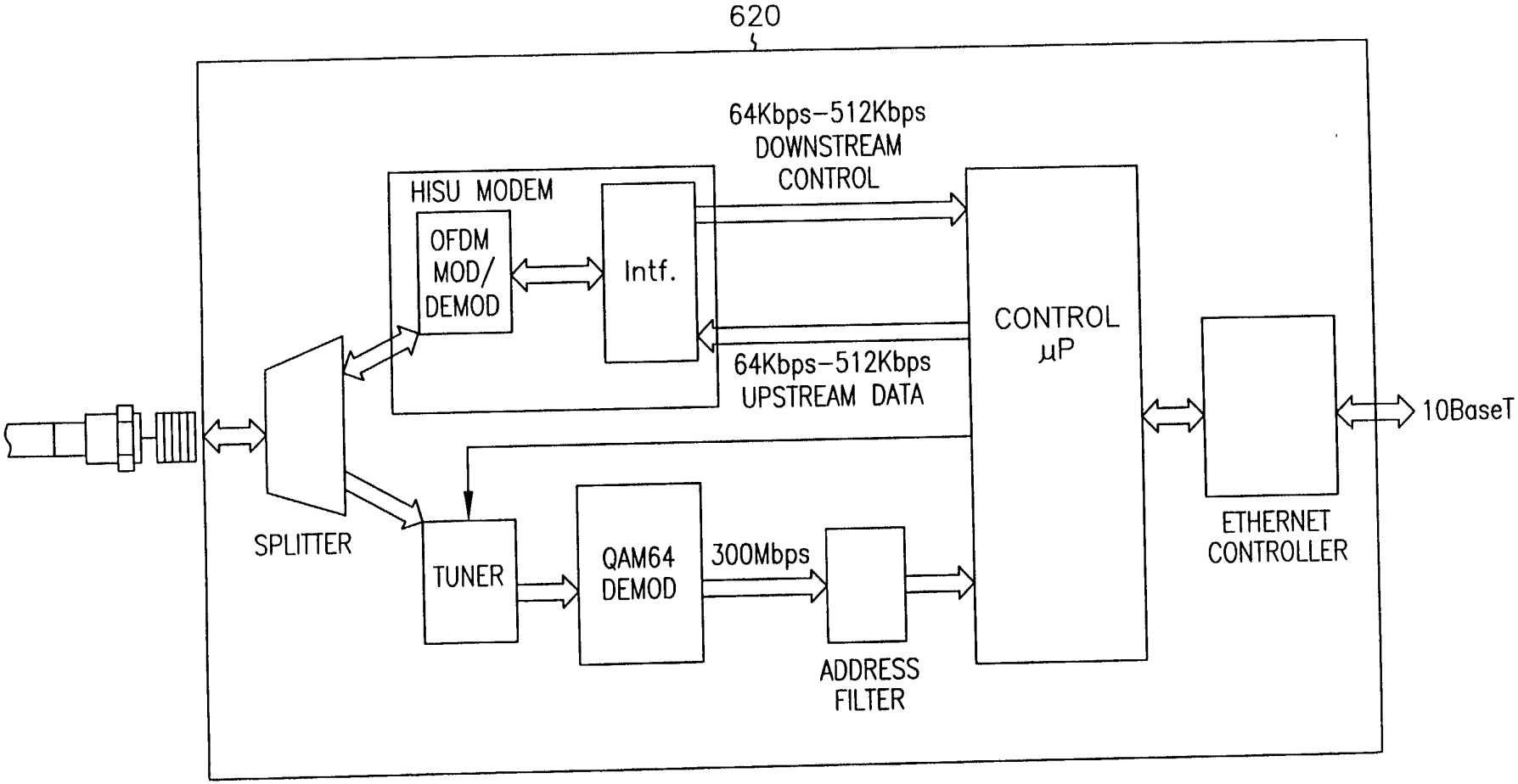


FIG. 112

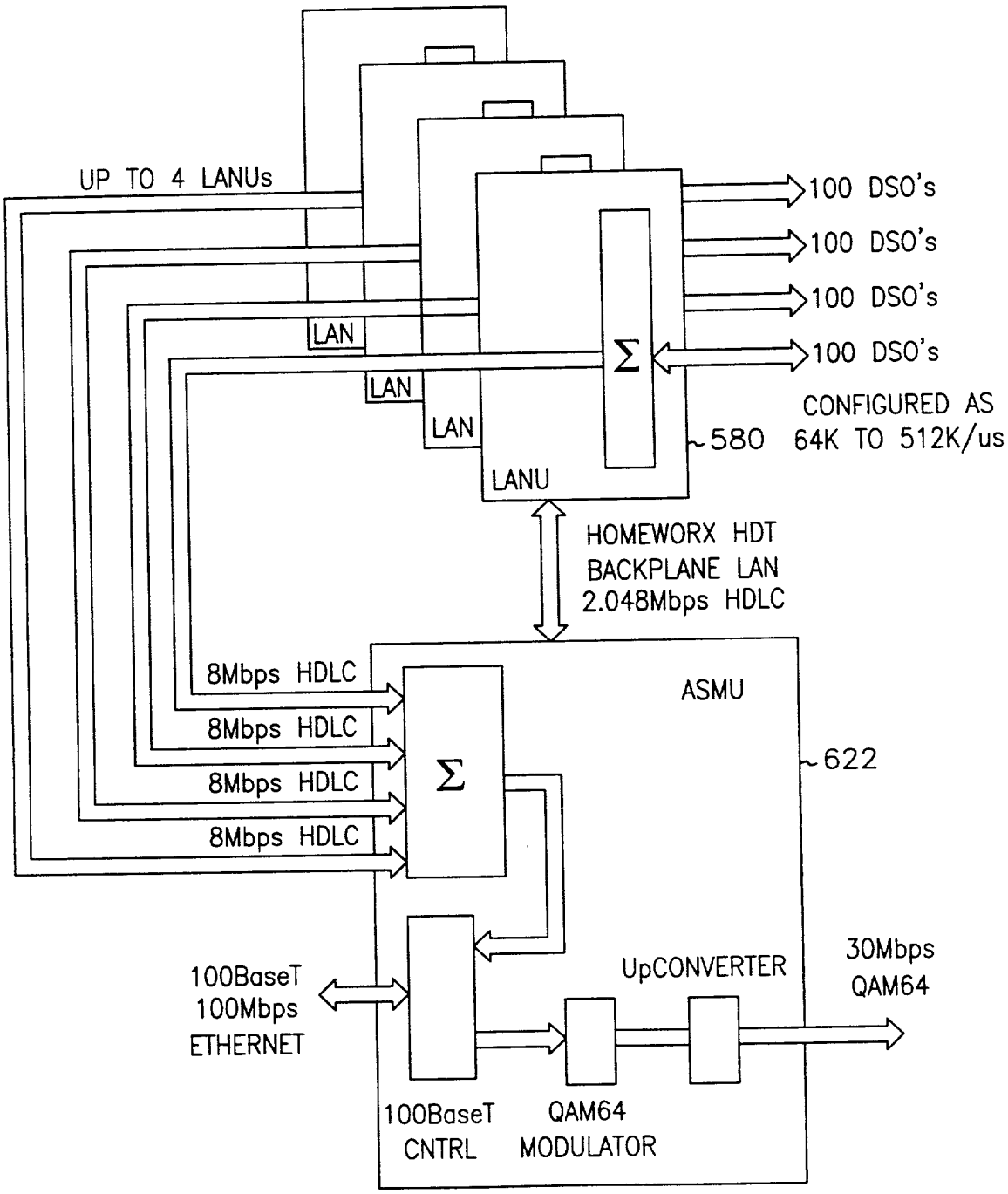

UP TO 4 LANUs
100 DSO's
100 DSO's
100 DSO's
100 DSO's
LAN
LAN
LAN
LANU
Σ
CONFIGURED AS
64K TO 512K/us
~580
HOMEWORX HDT
BACKPLANE LAN
2.048Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
8Mbps HDLC
Σ
ASMU
~622
100BaseT
100Mbps
ETHERNET
UpCONVERTER
30Mbps
QAM64
100BaseT
CNTRL
QAM64
MODULATOR

FIG. 113

SCREENSHOT

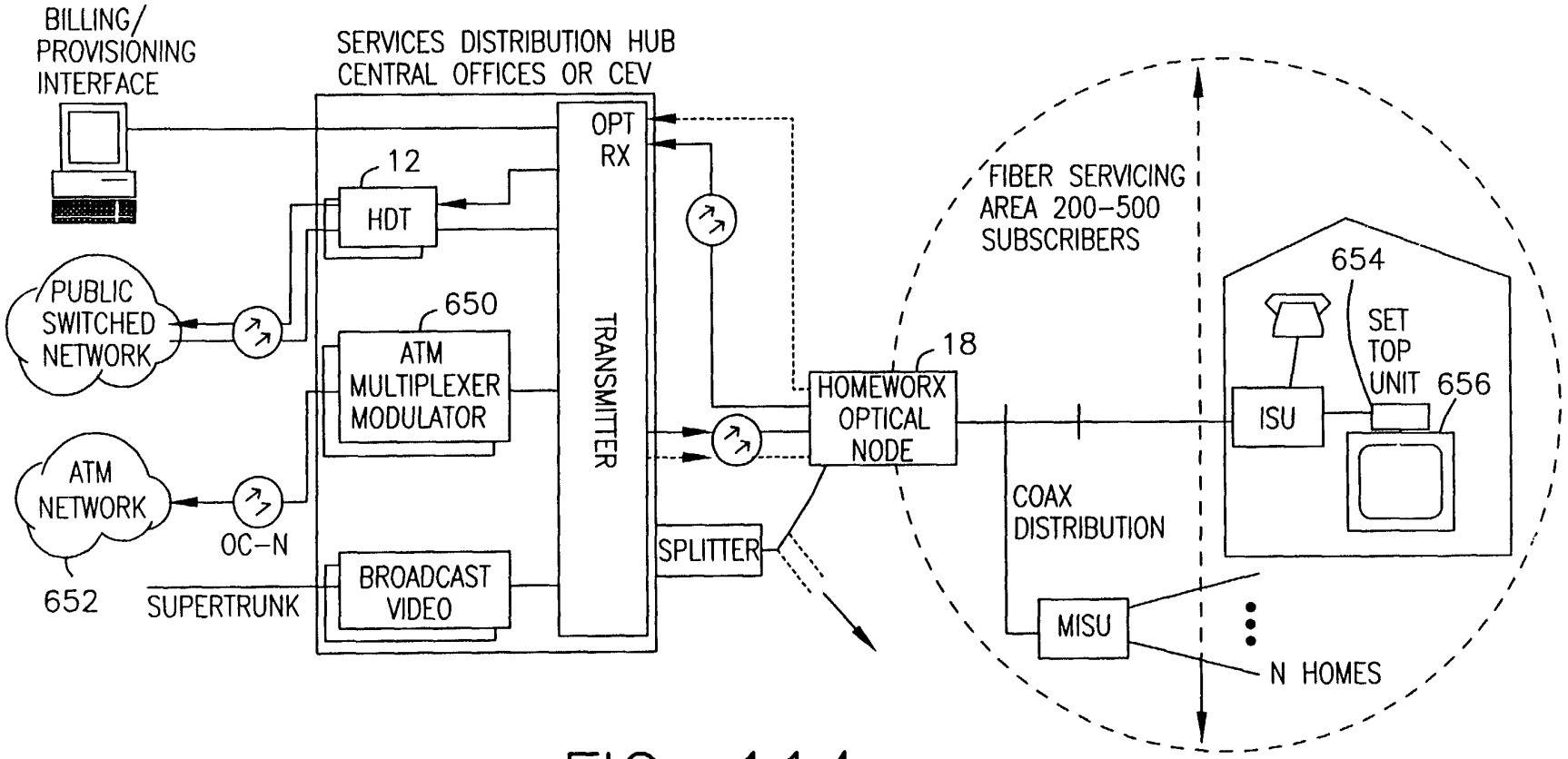


FIG. 114

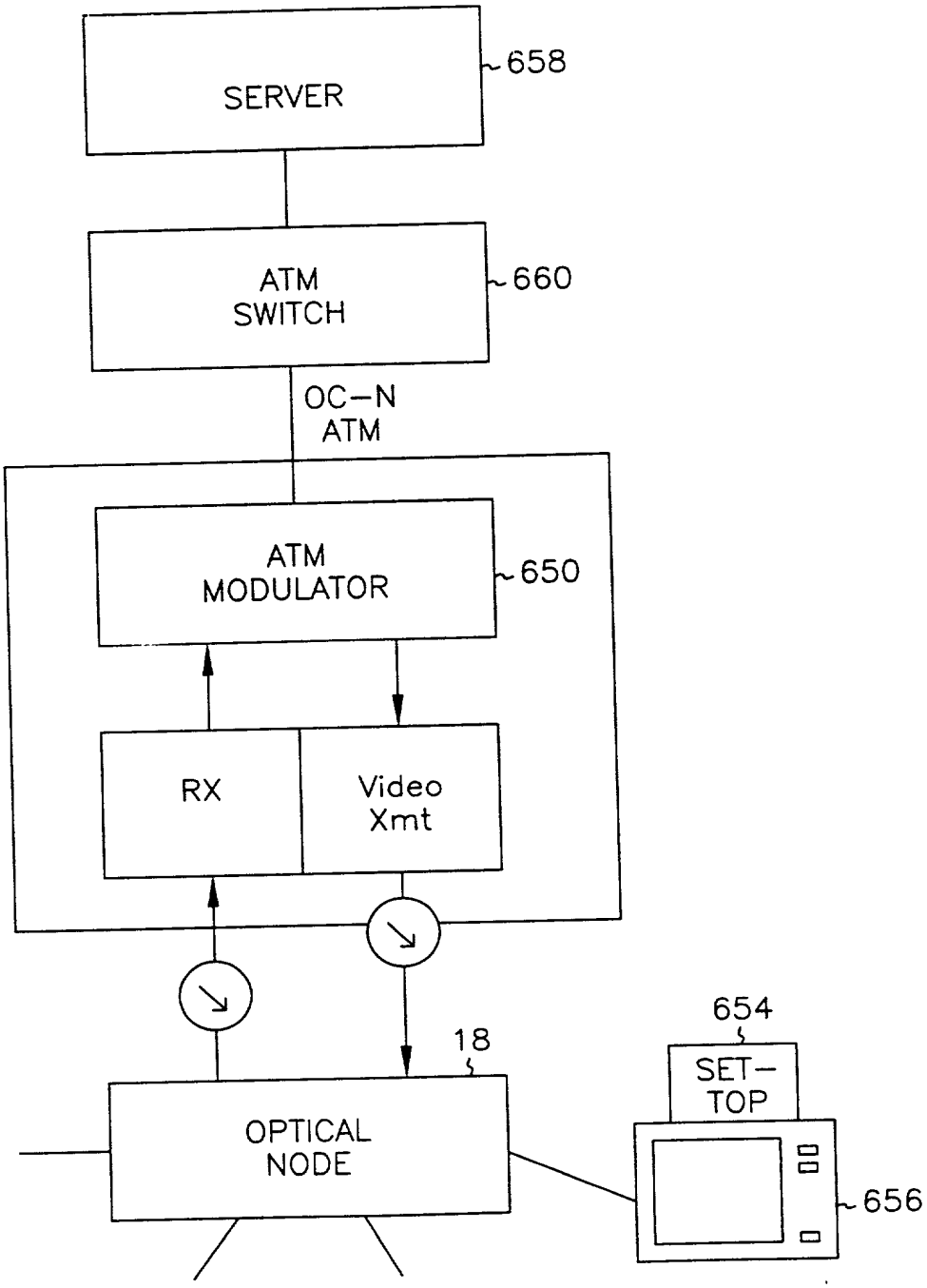

SERVER
658
ATM
SWITCH
660
OC–N
ATM
ATM
MODULATOR
650
RX
Video
Xmt
18
654
SET–
TOP
OPTICAL
NODE
656

FIG. 115

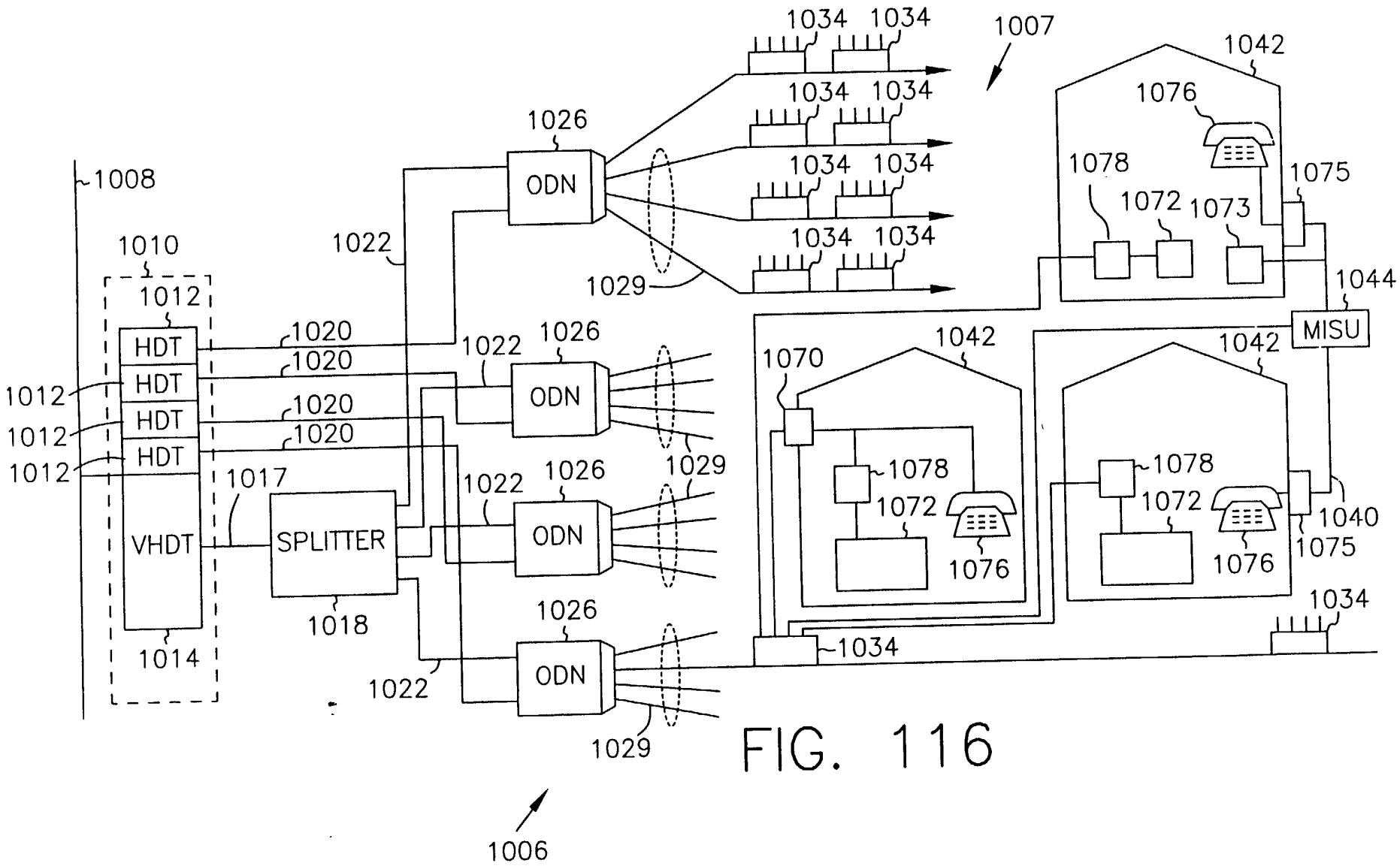

1008
1010
1012
HDT
HDT
HDT
HDT
VHDT
1014
1012
1012
1012
1020
1020
1020
1020
1017
SPLITTER
1018
1022
1022
1022
1026
ODN
1026
ODN
1026
ODN
1029
1029
1029
1034 1034
1034 1034
1034 1034
1034 1034
1007
1042
1076
1078
1072
1073
1075
1044
MISU
1042
1042
1070
1078
1072
1076
1078
1072
1076
1040
1075
1034
1034
1006

FIG. 116

SCANNED

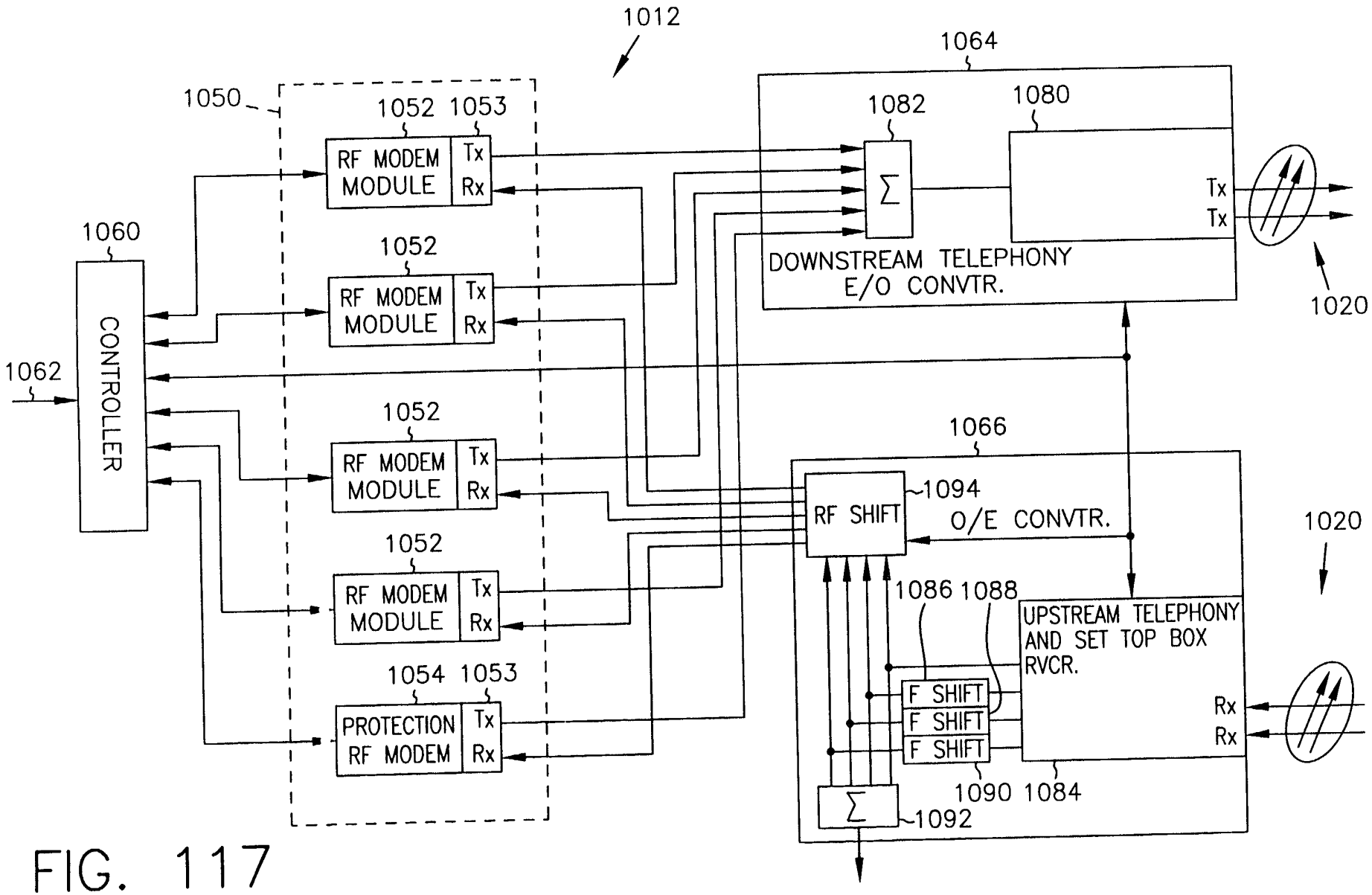


FIG. 117

EXHIBIT 1026

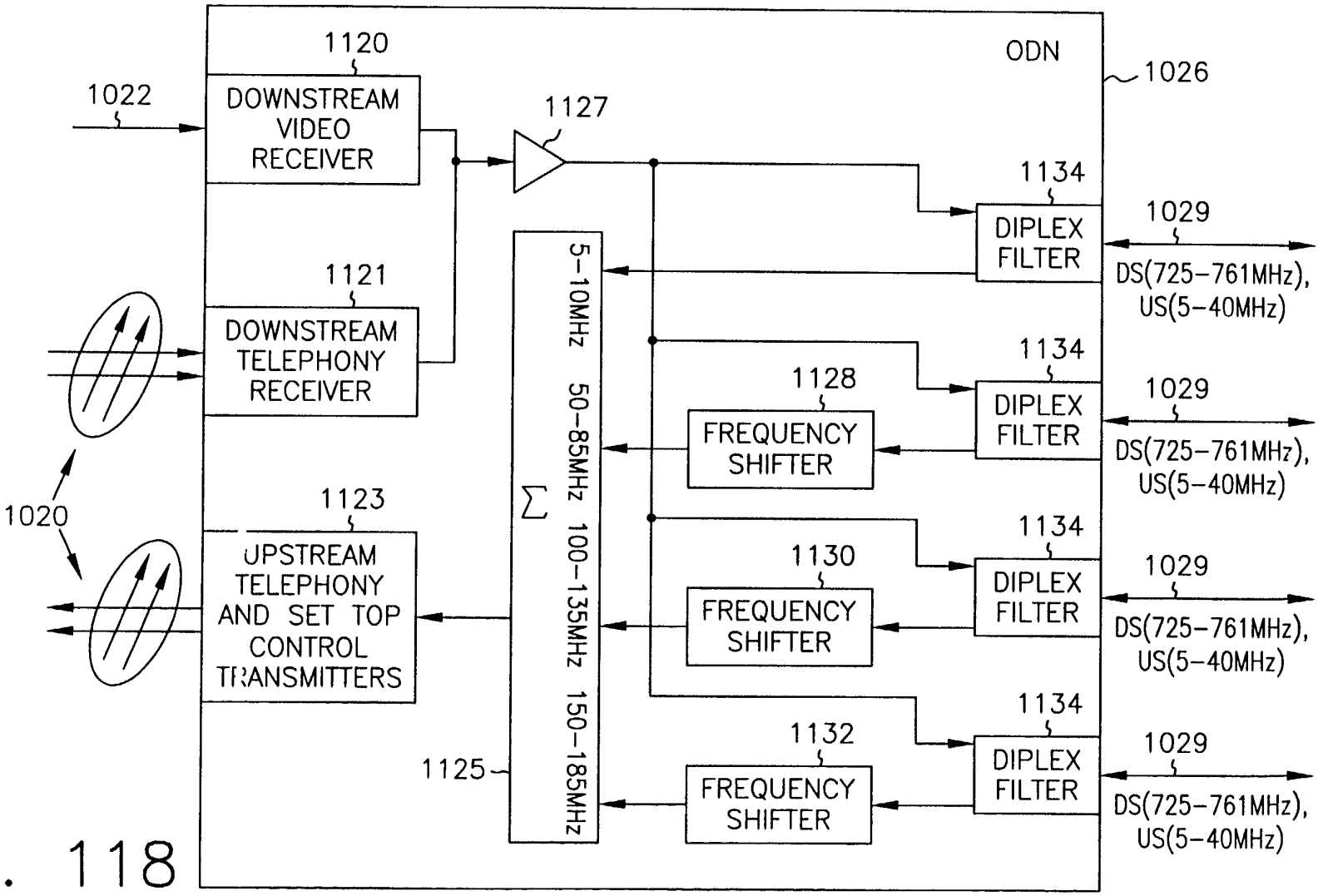


FIG. 118

20170105204007

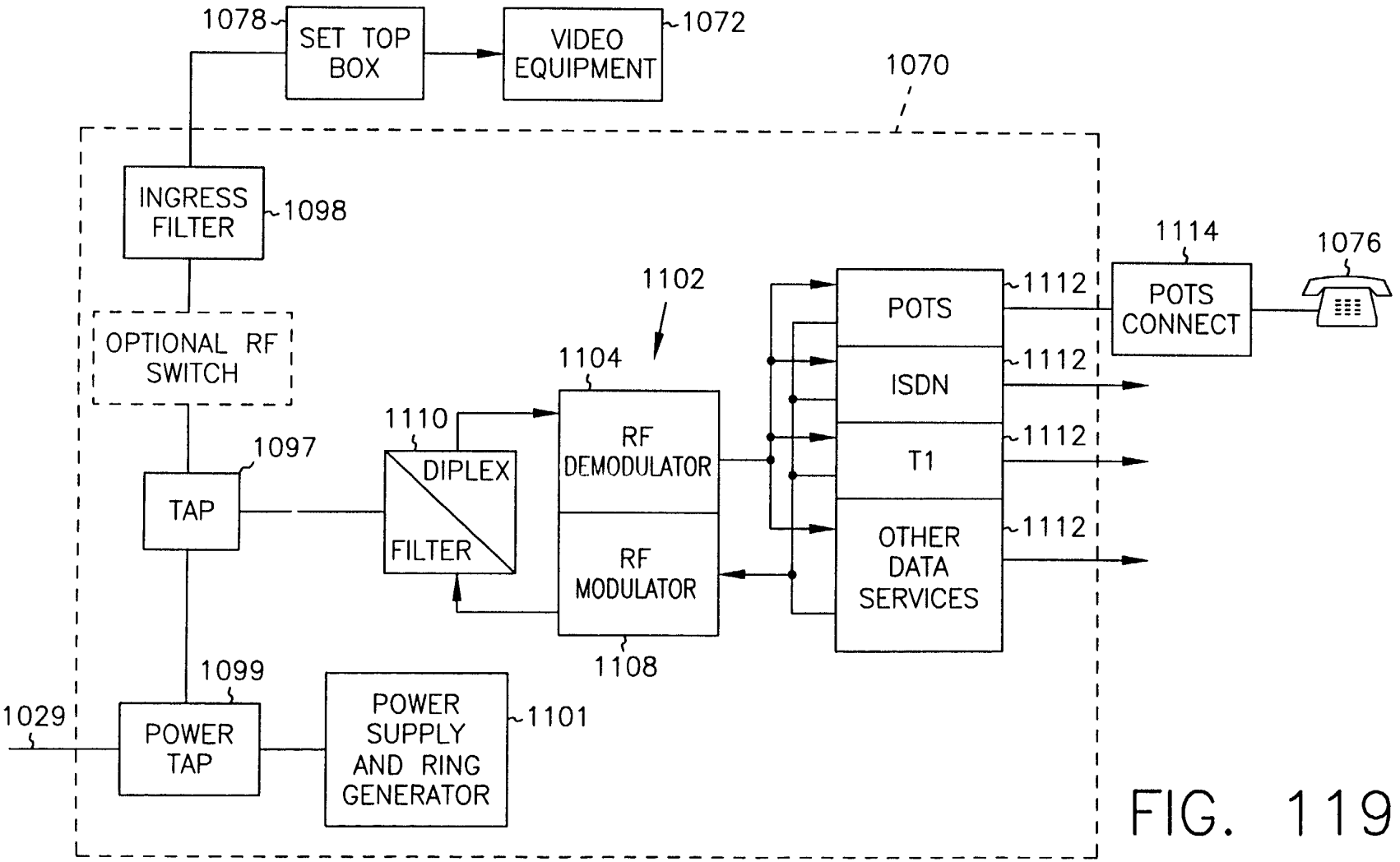


FIG. 119

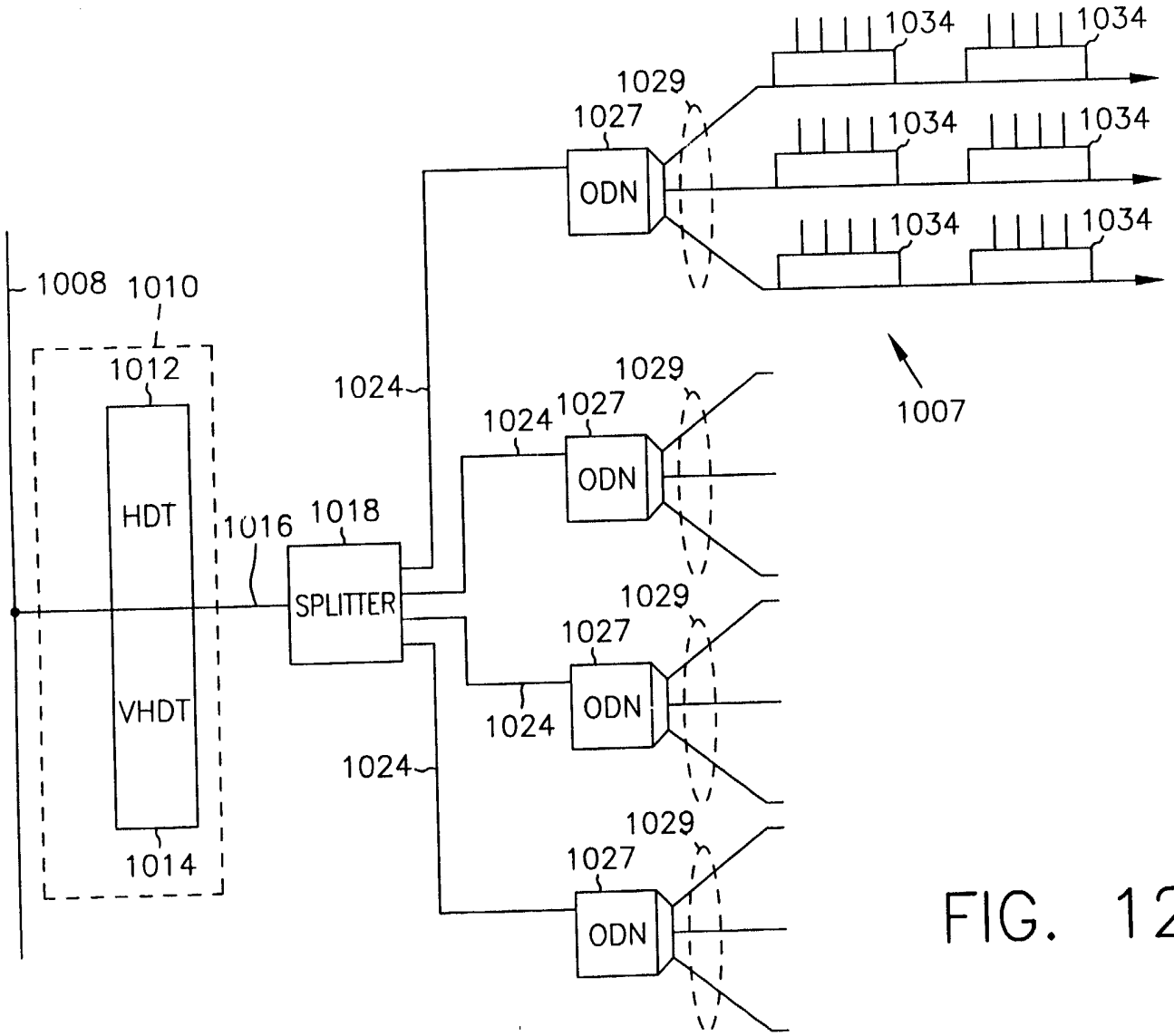

1034
1034
1029
1027
1034
1034
ODN
1034
1034
1008
1010
1012
1024
1029
1024
1027
ODN
1007
HDT
1016
1018
SPLITTER
1029
1027
VHDT
ODN
1024
1024
1029
1027
1014
ODN

FIG. 120

SCANNED BY SCANNER

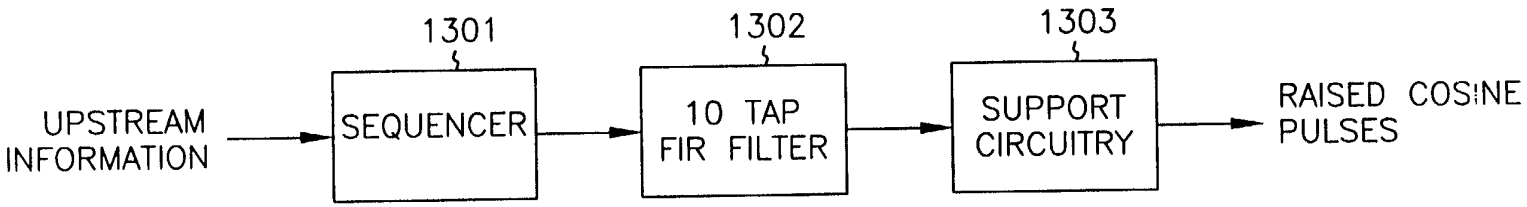


FIG. 121

SUBSTITUTE SHEET

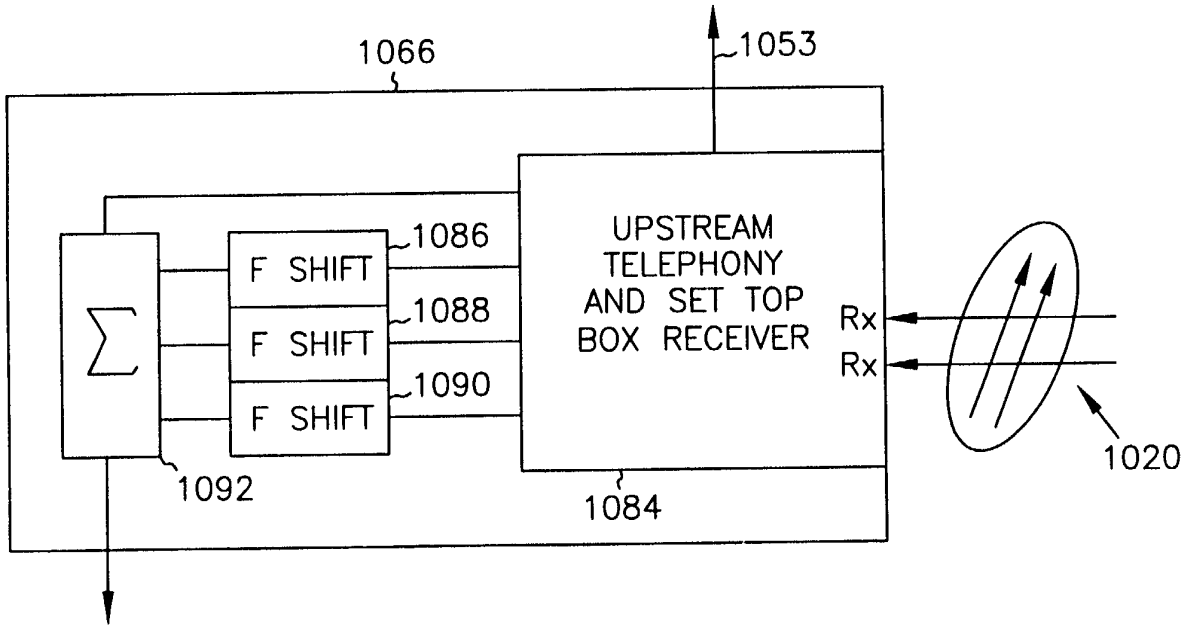


FIG. 122

Patent Application

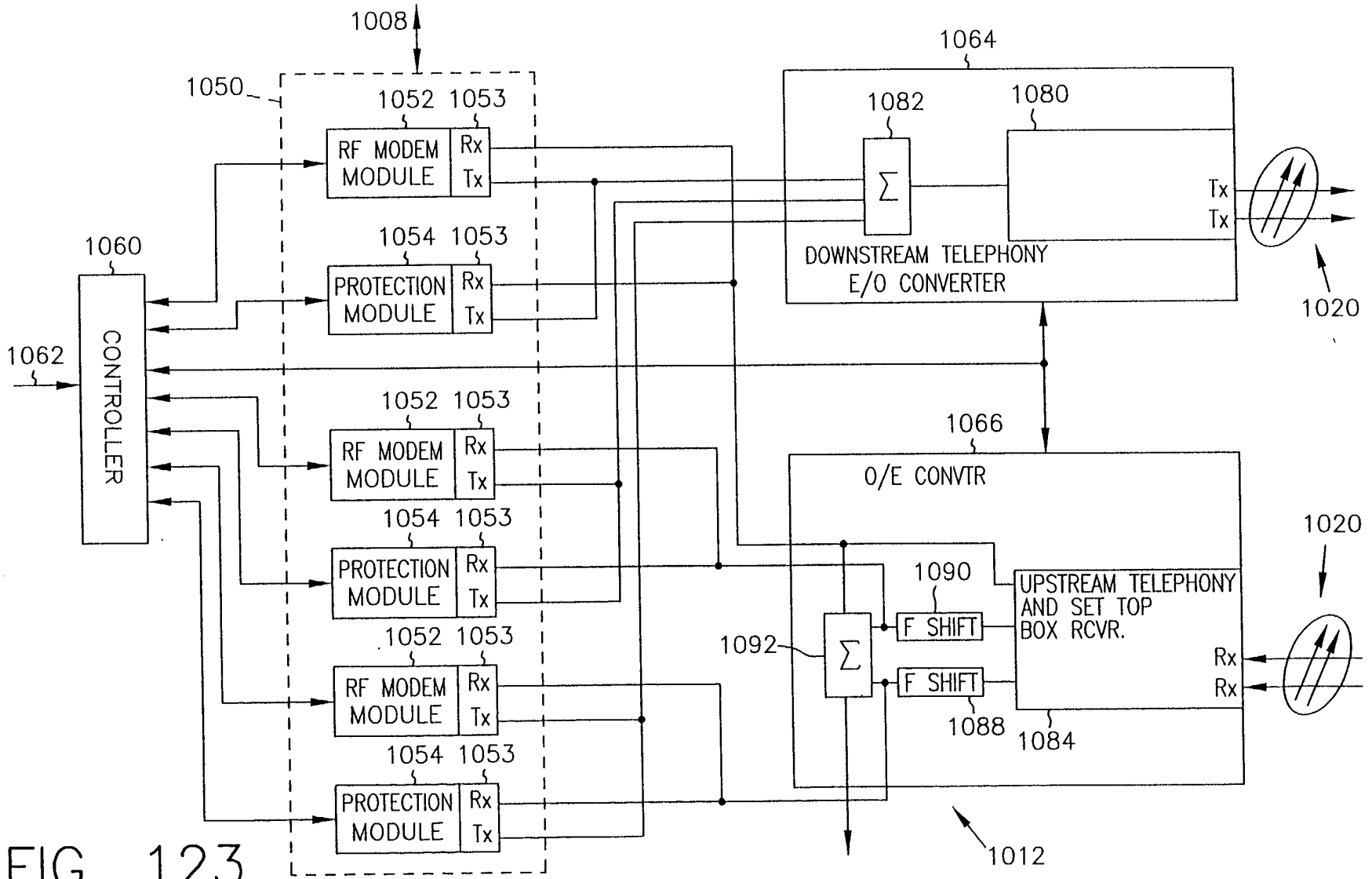


FIG. 123